



## TLV1117 Adjustable and Fixed Low-Dropout Voltage Regulator

### 1 Features

- 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V, and Adjustable-Output Voltage Options
- Output Current of 800 mA
- Specified Dropout Voltage at Multiple Current Levels
- 0.2% Line Regulation Maximum
- 0.4% Load Regulation Maximum

### 2 Applications

- Electronic Points of Sale
- Medical, Health, and Fitness Applications
- Printers
- Appliances and White Goods
- TV Set-Top Boxes

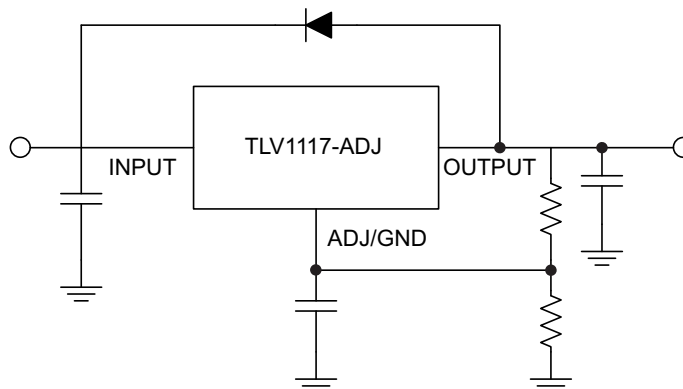
### 3 Description

The TLV1117 device is a positive low-dropout voltage regulator designed to provide up to 800 mA of output current. The device is available in 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V, and adjustable-output voltage options. All internal circuitry is designed to operate down to 1-V input-to-output differential. Dropout voltage is specified at a maximum of 1.3 V at 800 mA, decreasing at lower load currents.

#### Device Information

ORDER NUMBER	PACKAGE (PIN)	BODY SIZE
TLV1117DCY	SOT-223 (4)	6.50 mm × 3.50 mm
TLV1117DRJ	SON (8)	4.00 mm × 4.00 mm
TLV1117KVU	TO-252 (3)	6.60 mm × 6.10 mm
TLV1117KCS	TO-220 (3)	10.16 mm × 8.70 mm
TLV1117KCT	TO-220 (3)	10.16 mm × 8.59 mm
TLV1117KTT	DDPAK, TO-263 (3)	10.18 mm × 8.41 mm

### 4 Simplified Schematic



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### Changes from Revision K (April 2013) to Revision L

**Page**

• Updated data sheet to new TI standards – no specification changes. ....	<b>1</b>
• Deleted Ordering Information table. ....	<b>1</b>
• Added Applications. ....	<b>1</b>
• Added Device and Documentation Support section. ....	<b>14</b>
• Added Mechanical, Packaging, and Orderable Information section. ....	<b>14</b>

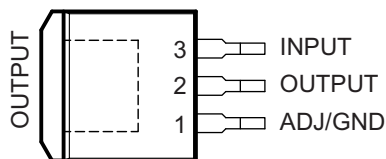
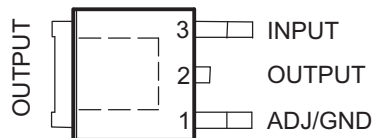
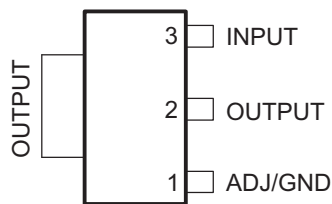
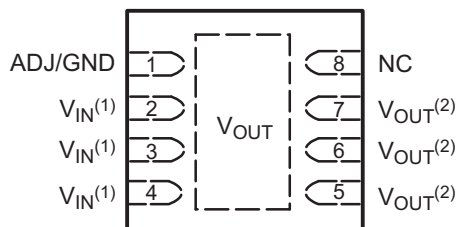
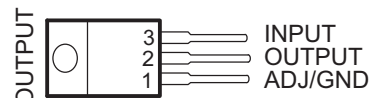
## 5 Revision History

### Changes from Revision J (April 2013) to Revision K

**Page**

• Added additional package options. ....	<b>3</b>
• Added ESD warning. ....	<b>14</b>

## 6 Pin Configuration and Functions

**KTT (TO-263) PACKAGE  
(TOP VIEW)**

**KVU (TO-252) PACKAGE  
(TOP VIEW)**

**DCY (SOT-223) PACKAGE  
(TOP VIEW)**

**DRJ (QFN) PACKAGE  
(TOP VIEW)**

**KCT, KCS (TO-220) PACKAGE  
(TOP VIEW)**


(1)  $V_{IN}$  pins (2, 3, 4) must be connected together.  
 (2)  $V_{OUT}$  pins (5, 6, 7) must be connected together.

**Table 1. Pin Functions**

NAME	PIN					TYPE	DESCRIPTION
	KTT	KVU	DCY	DRJ	KCT		
ADJ/GND	1	1	1	1	1	I/O	Output voltage adjustment pin. Connect to a resistor divider.
INPUT	3	3	3	2, 3, 4	3	I	Voltage input
OUTPUT	2	2	2	5, 6, 7	2	O	Voltage output
NC	-	-	-	8	-	-	No connect

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>IN</sub>	Continuous input voltage		16	V
T <sub>J</sub>	Operating virtual-junction temperature		150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 Handling Ratings

		MIN	MAX	UNIT	
T <sub>stg</sub>	Storage temperature range	–65	150	°C	
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	0	2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	0	1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

		MIN <sup>(1)</sup>	MAX	UNIT	
V <sub>IN</sub>	Input voltage	TLV1117	2.7	15	V
		TLV1117-15	2.9	15	
		TLV1117-18	3.2	15	
		TLV1117-25	3.9	15	
		TLV1117-33	4.7	15	
		TLV1117-50	6.4	15	
I <sub>O</sub>	Output current		0.8	A	
T <sub>J</sub>	Operating virtual-junction temperature	TLV1117C	0	125	°C
		TLV1117I	–40	125	

- (1) The input-to-output differential across the regulator should provide for some margin against regulator operation at the maximum dropout (for a particular current value). This margin is needed to account for tolerances in both the input voltage (lower limit) and the output voltage (upper limit). The absolute minimum V<sub>IN</sub> for a desired maximum output current can be calculated by the following:

$$V_{IN(\min)} = V_{OUT(\max)} + V_{DO(\max \text{ at rated current})}$$

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)(2)(3)</sup>		TLV1117							UNITS
		PowerFlex		DRJ (8 PINS)	DCY (4 PINS)	KVU (3 PINS)	KCS, KCT (3 PINS)	KTT (3 PINS)	
		KTE (3 PINS)	KTP (3 PINS)						
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	38.6	49.2	38.3	104.3	50.9	30.1	27.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	34.7	60.6	36.5	53.7	57.9	44.6	43.2	
R <sub>θJB</sub>	Junction-to-board thermal resistance	3.2	3.1	60.5	5.7	34.8	1.2	17.3	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	5.9	8.7	0.2	3.1	6	5	2.8	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	3.1	3	12	5.5	23.7	1.2	9.3	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	3	3	4.7	n/a	0.4	0.4	0.3	
R <sub>θJP</sub>	Thermal resistance between the die junction and the bottom of the exposed pad.	2.7	1.4	1.78	n/a	n/a	3	1.94	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) For thermal estimates of this device based on PCB copper area, see the [TI PCB Thermal Calculator](#).
- (3) Maximum power dissipation is a function of T<sub>J(max)</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> – T<sub>A</sub>) / θ<sub>JA</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.

## 7.5 TLV1117C Electrical Characteristics

$T_J = 0^\circ\text{C}$  to  $125^\circ\text{C}$ , all typical values are at  $T_J = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>	MIN	TYP	MAX	UNIT	
Reference voltage, $V_{REF}$	$V_{IN} - V_{OUT} = 2\text{ V}$ , $I_{OUT} = 10\text{ mA}$ , $T_J = 25^\circ\text{C}$	1.238	1.25	1.262	V	
	$V_{IN} - V_{OUT} = 1.4\text{ V to }10\text{ V}$ , $I_{OUT} = 10\text{ mA to }800\text{ mA}$	1.225	1.25	1.27		
Output voltage, $V_{OUT}$	$V_{IN} = 3.5\text{ V}$ , $I_{OUT} = 10\text{ mA}$ , $T_J = 25^\circ\text{C}$	1.485	1.5	1.515		
	$V_{IN} = 2.9\text{ V to }10\text{ V}$ , $I_{OUT} = 0\text{ to }800\text{ mA}$	1.455	1.5	1.545		
	$V_{IN} = 3.8\text{ V}$ , $I_{OUT} = 10\text{ mA}$ , $T_J = 25^\circ\text{C}$	1.782	1.8	1.818		
	$V_{IN} = 3.2\text{ V to }10\text{ V}$ , $I_{OUT} = 0\text{ to }800\text{ mA}$	1.746	1.8	1.854		
	$V_{IN} = 4.5\text{ V}$ , $I_{OUT} = 10\text{ mA}$ , $T_J = 25^\circ\text{C}$	2.475	2.5	2.525		
	$V_{IN} = 3.9\text{ V to }10\text{ V}$ , $I_{OUT} = 0\text{ to }800\text{ mA}$	2.450	2.5	2.550		
	$V_{IN} = 5\text{ V}$ , $I_{OUT} = 10\text{ mA}$ , $T_J = 25^\circ\text{C}$	3.267	3.3	3.333		
	$V_{IN} = 4.75\text{ V to }10\text{ V}$ , $I_{OUT} = 0\text{ to }800\text{ mA}$	3.235	3.3	3.365		
	$V_{IN} = 7\text{ V}$ , $I_{OUT} = 10\text{ mA}$ , $T_J = 25^\circ\text{C}$	4.950	5.0	5.050		
	$V_{IN} = 6.5\text{ V to }12\text{ V}$ , $I_{OUT} = 0\text{ to }800\text{ mA}$	4.900	5.0	5.100		
Line regulation	$I_{OUT} = 10\text{ mA}$ , $V_{IN} - V_{OUT} = 1.5\text{ V to }13.75\text{ V}$		0.035%	0.2%		—
	$I_{OUT} = 0\text{ mA}$ , $V_{IN} = 2.9\text{ V to }10\text{ V}$		1	6		mV
	$I_{OUT} = 0\text{ mA}$ , $V_{IN} = 3.2\text{ V to }10\text{ V}$		1	6		
	$I_{OUT} = 0\text{ mA}$ , $V_{IN} = 3.9\text{ V to }10\text{ V}$		1	6		
	$I_{OUT} = 0\text{ mA}$ , $V_{IN} = 4.75\text{ V to }15\text{ V}$		1	6		
	$I_{OUT} = 0\text{ mA}$ , $V_{IN} = 6.5\text{ V to }15\text{ V}$		1	10		
Load regulation	$I_{OUT} = 10\text{ mA to }800\text{ mA}$ , $V_{IN} - V_{OUT} = 3\text{ V}$		0.2%	0.4%	—	
	$I_{OUT} = 0\text{ to }800\text{ mA}$ , $V_{IN} = 2.9\text{ V}$		1	10	mV	
	$I_{OUT} = 0\text{ to }800\text{ mA}$ , $V_{IN} = 3.2\text{ V}$		1	10		
	$I_{OUT} = 0\text{ to }800\text{ mA}$ , $V_{IN} = 3.9\text{ V}$		1	10		
	$I_{OUT} = 0\text{ to }800\text{ mA}$ , $V_{IN} = 4.75\text{ V}$		1	10		
	$I_{OUT} = 0\text{ to }800\text{ mA}$ , $V_{IN} = 6.5\text{ V}$		1	15		
Dropout voltage, $V_{DO}$ <sup>(2)</sup>	$I_{OUT} = 100\text{ mA}$		1.1	1.2		V
	$I_{OUT} = 500\text{ mA}$		1.15	1.25		
	$I_{OUT} = 800\text{ mA}$		1.2	1.3		
Current limit	$V_{IN} - V_{OUT} = 5\text{ V}$ , $T_J = 25^\circ\text{C}$ <sup>(3)</sup>	0.8	1.2	1.6	A	
Minimum load current	$V_{IN} = 15\text{ V}$		1.7	5	mA	
Quiescent current	$V_{IN} \leq 15\text{ V}$		5	10	mA	
Thermal regulation	30-ms pulse, $T_A = 25^\circ\text{C}$		0.01	0.1	%/W	
Ripple rejection	$V_{IN} - V_{OUT} = 3\text{ V}$ , $V_{ripple} = 1\text{ V}_{pp}$ , $f = 120\text{ Hz}$	60	75		dB	
ADJ pin current			80	120	$\mu\text{A}$	
Change in ADJ pin current	$V_{IN} - V_{OUT} = 1.4\text{ V to }10\text{ V}$ , $I_{OUT} = 10\text{ mA to }800\text{ mA}$		0.2	5	$\mu\text{A}$	
Temperature stability	$T_J = \text{full range}$		0.5%		—	
Long-term stability	1000 hrs, No load, $T_A = 125^\circ\text{C}$		0.3%		—	
Output noise voltage (% of $V_{OUT}$ )	$f = 10\text{ Hz to }100\text{ kHz}$		0.003%		—	

- (1) All characteristics are measured with a 10- $\mu\text{F}$  capacitor across the input and a 10- $\mu\text{F}$  capacitor across the output. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible.
- (2) Dropout is defined as the  $V_{IN}$  to  $V_{OUT}$  differential at which  $V_{OUT}$  drops 100 mV below the value of  $V_{OUT}$ , measured at  $V_{IN} = V_{OUT(nom)} + 1.5\text{ V}$ .
- (3) Current limit test specified under recommended operating conditions.

## 7.6 TLV1117I Electrical Characteristics

 $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , all typical values are at  $T_J = 25^{\circ}\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>	MIN	TYP	MAX	UNIT	
Reference voltage, $V_{REF}$	$V_{IN} - V_{OUT} = 2\text{ V}$ , $I_{OUT} = 10\text{ mA}$ , $T_J = 25^{\circ}\text{C}$	1.238	1.25	1.262	V	
	$V_{IN} - V_{OUT} = 1.4\text{ V}$ to $10\text{ V}$ , $I_{OUT} = 10\text{ mA}$ to $800\text{ mA}$	1.200	1.25	1.29		
Output voltage, $V_{OUT}$	$V_{IN} = 3.5\text{ V}$ , $I_{OUT} = 10\text{ mA}$ , $T_J = 25^{\circ}\text{C}$	1.485	1.5	1.515		
	$V_{IN} = 2.9\text{ V}$ to $10\text{ V}$ , $I_{OUT} = 0$ to $800\text{ mA}$	1.44	1.5	1.56		
	$V_{IN} = 3.8\text{ V}$ , $I_{OUT} = 10\text{ mA}$ , $T_J = 25^{\circ}\text{C}$	1.782	1.8	1.818		
	$V_{IN} = 3.2\text{ V}$ to $10\text{ V}$ , $I_{OUT} = 0$ to $800\text{ mA}$	1.728	1.8	1.872		
	$V_{IN} = 4.5\text{ V}$ , $I_{OUT} = 10\text{ mA}$ , $T_J = 25^{\circ}\text{C}$	2.475	2.5	2.525		
	$V_{IN} = 3.9\text{ V}$ to $10\text{ V}$ , $I_{OUT} = 0$ to $800\text{ mA}$	2.4	2.5	2.6		
	$V_{IN} = 5\text{ V}$ , $I_{OUT} = 10\text{ mA}$ , $T_J = 25^{\circ}\text{C}$	3.267	3.3	3.333		
	$V_{IN} = 4.75\text{ V}$ to $10\text{ V}$ , $I_{OUT} = 0$ to $800\text{ mA}$	3.168	3.3	3.432		
	$V_{IN} = 7\text{ V}$ , $I_{OUT} = 10\text{ mA}$ , $T_J = 25^{\circ}\text{C}$	4.95	5.0	5.05		
	$V_{IN} = 6.5\text{ V}$ to $12\text{ V}$ , $I_{OUT} = 0$ to $800\text{ mA}$	4.80	5.0	5.20		
Line regulation	$I_{OUT} = 10\text{ mA}$ , $V_{IN} - V_{OUT} = 1.5\text{ V}$ to $13.75\text{ V}$		0.035%	0.3%		—
	$I_{OUT} = 0\text{ mA}$ , $V_{IN} = 2.9\text{ V}$ to $10\text{ V}$		1	10		mV
	$I_{OUT} = 0\text{ mA}$ , $V_{IN} = 3.2\text{ V}$ to $10\text{ V}$		1	10		
	$I_{OUT} = 0\text{ mA}$ , $V_{IN} = 3.9\text{ V}$ to $10\text{ V}$		1	10		
	$I_{OUT} = 0\text{ mA}$ , $V_{IN} = 4.75\text{ V}$ to $15\text{ V}$		1	10		
	$I_{OUT} = 0\text{ mA}$ , $V_{IN} = 6.5\text{ V}$ to $15\text{ V}$		1	15		
Load regulation	$I_{OUT} = 10\text{ mA}$ to $800\text{ mA}$ , $V_{IN} - V_{OUT} = 3\text{ V}$		0.2%	0.5%	—	
	$I_{OUT} = 0$ to $800\text{ mA}$ , $V_{IN} = 2.9\text{ V}$		1	15	mV	
	$I_{OUT} = 0$ to $800\text{ mA}$ , $V_{IN} = 3.2\text{ V}$		1	15		
	$I_{OUT} = 0$ to $800\text{ mA}$ , $V_{IN} = 3.9\text{ V}$		1	15		
	$I_{OUT} = 0$ to $800\text{ mA}$ , $V_{IN} = 4.75\text{ V}$		1	15		
	$I_{OUT} = 0$ to $800\text{ mA}$ , $V_{IN} = 6.5\text{ V}$		1	20		
Dropout voltage, $V_{DO}$ <sup>(2)</sup>	$I_{OUT} = 100\text{ mA}$		1.1	1.3		V
	$I_{OUT} = 500\text{ mA}$		1.15	1.35		
	$I_{OUT} = 800\text{ mA}$		1.2	1.4		
Current limit	$V_{IN} - V_{OUT} = 5\text{ V}$ , $T_J = 25^{\circ}\text{C}$ <sup>(3)</sup>	0.8	1.2	1.6	A	
Minimum load current	$V_{IN} = 15\text{ V}$		1.7	5	mA	
Quiescent current	$V_{IN} \leq 15\text{ V}$		5	15	mA	
Thermal regulation	30-ms pulse, $T_A = 25^{\circ}\text{C}$		0.01	0.1	%/W	
Ripple rejection	$V_{IN} - V_{OUT} = 3\text{ V}$ , $V_{ripple} = 1\text{ V}_{pp}$ , $f = 120\text{ Hz}$	60	75		dB	
ADJ pin current			80	120	$\mu\text{A}$	
Change in ADJ pin current	$V_{IN} - V_{OUT} = 1.4\text{ V}$ to $10\text{ V}$ , $I_{OUT} = 10\text{ mA}$ to $800\text{ mA}$		0.2	10	$\mu\text{A}$	
Temperature stability	$T_J = \text{full range}$		0.5%		—	
Long-term stability	1000 hrs, No load, $T_A = 125^{\circ}\text{C}$		0.3%		—	
Output noise voltage (% of $V_{OUT}$ )	$f = 10\text{ Hz}$ to $100\text{ kHz}$		0.003%		—	

- (1) All characteristics are measured with a 10- $\mu\text{F}$  capacitor across the input and a 10- $\mu\text{F}$  capacitor across the output. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible.
- (2) Dropout is defined as the  $V_{IN}$  to  $V_{OUT}$  differential at which  $V_{OUT}$  drops 100 mV below the value of  $V_{OUT}$ , measured at  $V_{IN} = V_{OUT(nom)} + 1.5\text{ V}$ .
- (3) Current limit test specified under recommended operating conditions

### 7.7 Typical Characteristics

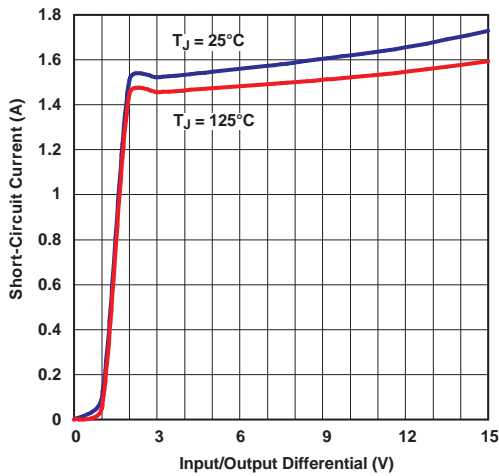


Figure 1. Short-Circuit Current vs ( $V_{IN} - V_{OUT}$ )

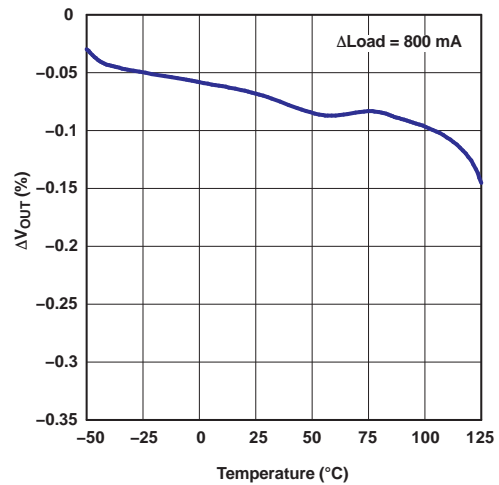


Figure 2. Load Regulation

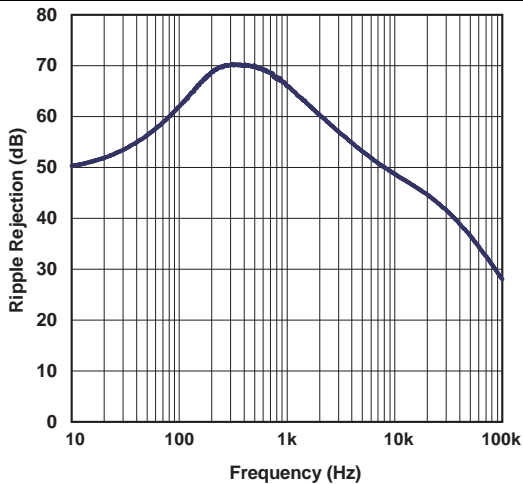


Figure 3. Ripple Rejection vs Frequency (ADJ Version)

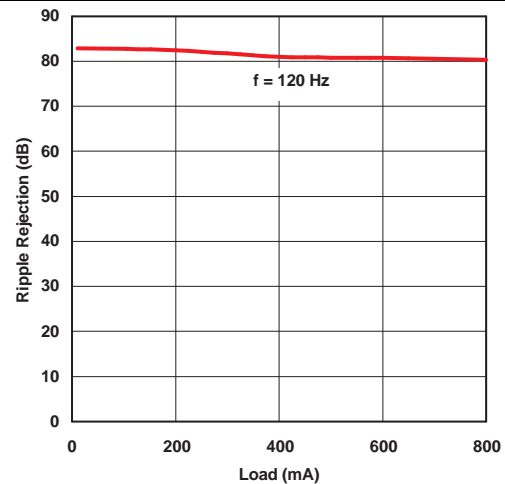


Figure 4. Ripple Rejection vs Load Current (ADJ Version)

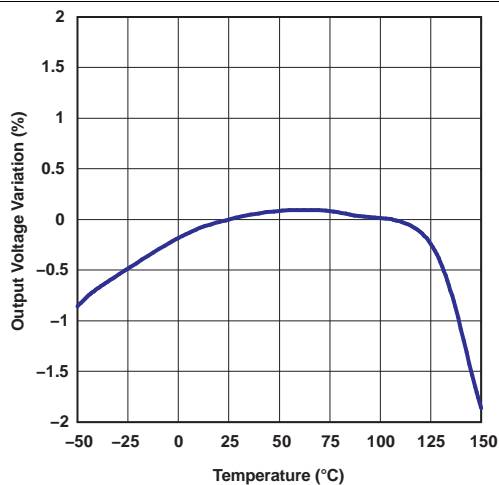


Figure 5. Temperature Stability

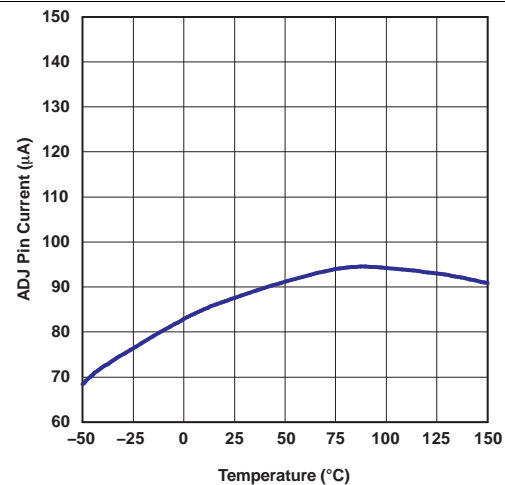
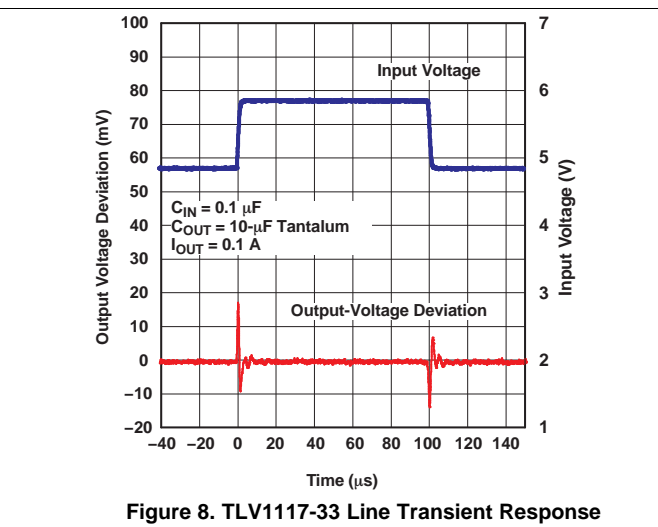
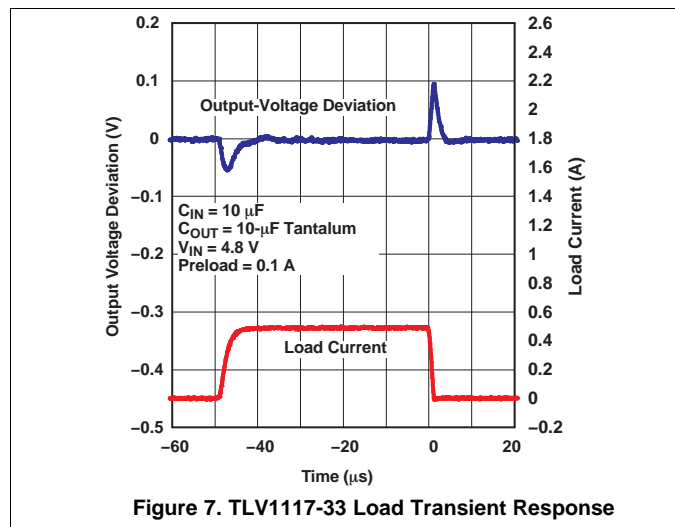


Figure 6. ADJ Pin Current vs Temperature



Typical Characteristics (continued)



## 8 Detailed Description

### 8.1 Overview

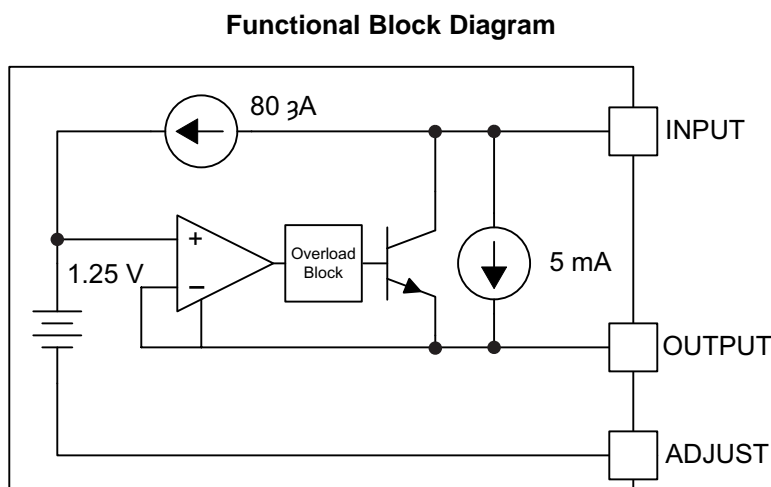
The TLV1117 device is a positive low-dropout voltage regulator designed to provide up to 800 mA of output current. The device is available in 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V, and adjustable-output voltage options. All internal circuitry is designed to operate down to 1-V input-to-output differential. Dropout voltage is specified at a maximum of 1.3 V at 800 mA, decreasing at lower load currents.

The TLV1117 device is designed to be stable with tantalum and aluminum electrolytic output capacitors having an ESR between 0.2 Ω and 10 Ω.

Unlike pnp-type regulators, in which up to 10% of the output current is wasted as quiescent current, the quiescent current of the TLV1117 device flows into the load, increasing efficiency.

The TLV1117C device is characterized for operation over the virtual junction temperature range of 0°C to 125°C, and the TLV1117I device is characterized for operation over the virtual junction temperature range of –40°C to 125°C.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 NPN Output Drive

NPN output topology provides lower output impedance than most LDOs. However, an output capacitor is required. To support maximum current and lowest temperature, 1.4-V headroom is recommended (less for lower currents) ( $V_I - V_O$ ).

#### 8.3.2 Overload Block

Current limiting and over temperature shutdown protects against overload or under heat sinking.

#### 8.3.3 Programmable Feedback

Op amp with 1.25-V offset input at the ADJUST pin provides easy output voltage programming. For current regulation applications, a single resistor whose resistance value is  $1.25 \text{ V} / I_{\text{OUT}}$  and power rating is greater than  $(1.25 \text{ V})^2 / R$  should be used. For voltage regulation applications, two resistors set the output voltage.

### 8.4 Device Functional Modes

#### 8.4.1 Normal operation

The device OUTPUT pin will source current necessary to make OUTPUT pin 1.25 V greater than ADJUST terminal to provide output regulation.

## Device Functional Modes (continued)

### 8.4.2 Operation With Low Input Voltage

The adjustable version of the device requires 1-V headroom ( $V_I - V_O$ ) to operate in regulation. With less headroom, the device may drop out and OUTPUT voltage will be INPUT voltage minus drop out voltage.

### 8.4.3 Operation at Light Loads

The device passes its bias current to the OUTPUT pin. The load or feedback must consume this minimum current for regulation or the output may be too high.

### 8.4.4 Operation in Self Protection

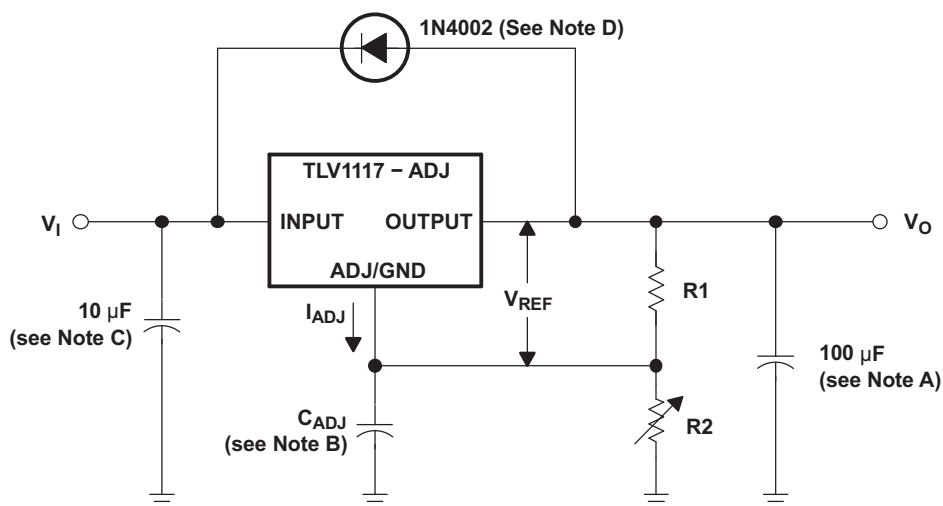
When an overload occurs the device will shut down the output stage or reduce the output current to prevent device damage. The device will automatically reset from the overload. The output may be reduced or alternate between on and off until the overload is removed.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Typical Application



**Figure 9. Basic Adjustable Regulator**

The adjustable version of the TLV1117 will take a 2.7 to 15-V input. The voltage  $V_{REF}$  refers to the voltage between the output and the ADJUST pin, typically 1.25 V. The  $V_{REF}$  voltage causes a current to flow across R1, which is the same current that will flow across R2 (minus the negligible 50- $\mu$ A  $I_{ADJ}$ ). Therefore, R2 can be adjusted to create a larger voltage drop from GND and set the output voltage. The output voltage equation is described in [Detailed Design Procedure](#).

#### 9.1.1 Design Requirements

- (A) Output capacitor selection is critical for regulator stability. Larger  $C_{OUT}$  values benefit the regulator by improving transient response and loop stability. This device is designed to be stable with tantalum and aluminum electrolytic output capacitors having an ESR between 0.2  $\Omega$  and 10  $\Omega$ .
- (B)  $C_{ADJ}$  can be used to improve ripple rejection. If  $C_{ADJ}$  is used, a  $C_{OUT}$  that is larger in value than  $C_{ADJ}$  must be used.
- (C)  $C_{IN}$  is recommended if TLV1117 device is not located near the power-supply filter.
- (D) An external diode is recommended to protect the regulator if the input instantaneously is shorted to GND.

#### 9.1.2 Detailed Design Procedure

The output voltage can be calculated as shown in [Figure 10](#):

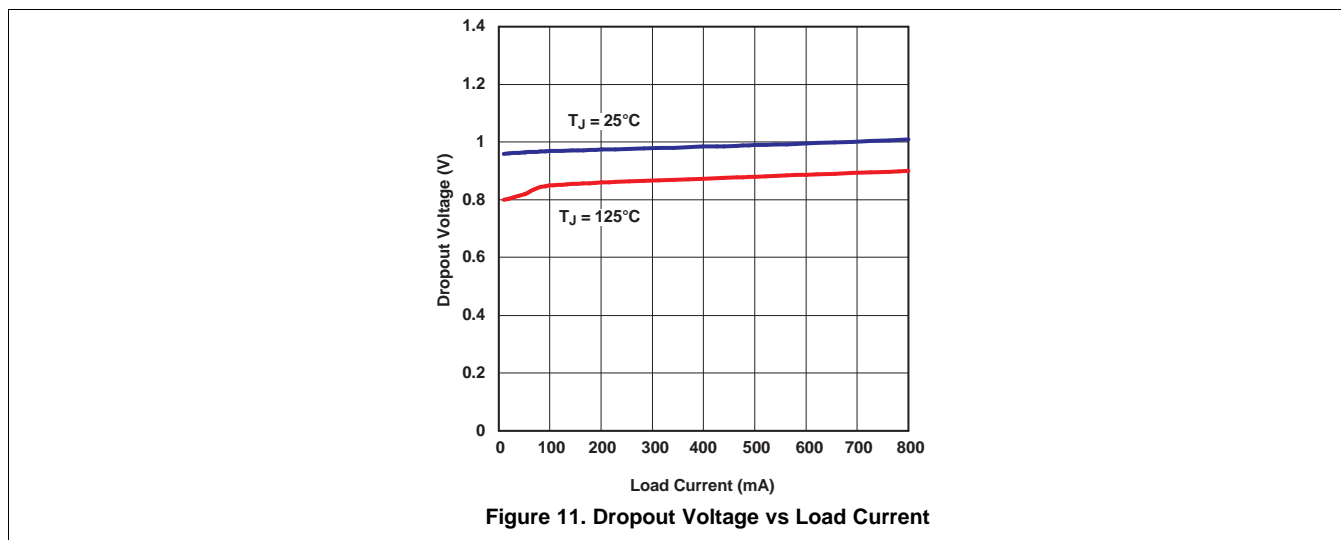
$$V_{OUT} = V_{REF} \left( 1 + \frac{R2}{R1} \right) + (I_{ADJ} \times R2)$$

**Figure 10.**

$I_{ADJ}$  can be neglected in most applications because its value is approximately 80  $\mu$ A.

## Typical Application (continued)

### 9.1.3 Application Curves



## 10 Power Supply Recommendations

The fixed and adjustable versions of the TLV1117 have different recommended ranges of operating voltage. Refer to [Recommended Operating Conditions](#) for specific operating ranges.

## 11 Layout

### 11.1 Layout Guidelines

One or two input capacitors are recommended if the TLV1117 is not located near its power supply output filter capacitor. These capacitors can filter high-frequency noise and mitigate brief voltage surges from the input. Traces on the input and output pins of the device should be wide enough to support the full range of current needed in the application to minimize  $I \times R$  drop.

### 11.2 Layout Example

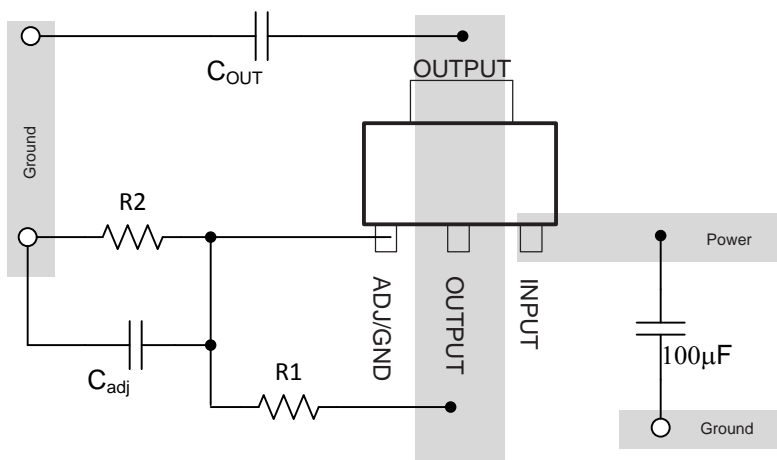


Figure 12. Layout Example

## 12 Device and Documentation Support

### 12.1 Trademarks

All trademarks are the property of their respective owners.

### 12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV1117-15CDCY	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	T2	<a href="#">Samples</a>
TLV1117-15CDCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	T2	<a href="#">Samples</a>
TLV1117-15CDCYRG3	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	T2	<a href="#">Samples</a>
TLV1117-15CDRJR	ACTIVE	SON	DRJ	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 125	ZYH	<a href="#">Samples</a>
TLV1117-15IDCY	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	T3	<a href="#">Samples</a>
TLV1117-15IDCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	T3	<a href="#">Samples</a>
TLV1117-15IKVURG3	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	ZF15	<a href="#">Samples</a>
TLV1117-18CDCY	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	T4	<a href="#">Samples</a>
TLV1117-18CDCYG3	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	T4	<a href="#">Samples</a>
TLV1117-18CDCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	T4	<a href="#">Samples</a>
TLV1117-18CDCYRG3	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	T4	<a href="#">Samples</a>
TLV1117-18CDRJR	ACTIVE	SON	DRJ	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 125	ZYK	<a href="#">Samples</a>
TLV1117-18CKVURG3	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	ZE18	<a href="#">Samples</a>
TLV1117-18IDCY	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	T5	<a href="#">Samples</a>
TLV1117-18IDCYG3	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	T5	<a href="#">Samples</a>
TLV1117-18IDCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	T5	<a href="#">Samples</a>
TLV1117-18IDCYRG3	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	T5	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV1117-18IDRJR	ACTIVE	SON	DRJ	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZYL	<a href="#">Samples</a>
TLV1117-18IKVURG3	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	ZF18	<a href="#">Samples</a>
TLV1117-25CDCY	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	T6	<a href="#">Samples</a>
TLV1117-25CDCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	T6	<a href="#">Samples</a>
TLV1117-25CDCYRG3	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	T6	<a href="#">Samples</a>
TLV1117-25CKVURG3	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	ZE25	<a href="#">Samples</a>
TLV1117-25IDCY	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	T8	<a href="#">Samples</a>
TLV1117-25IDCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	T8	<a href="#">Samples</a>
TLV1117-25IDRJR	ACTIVE	SON	DRJ	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZYN	<a href="#">Samples</a>
TLV1117-25IKCS	PREVIEW	TO-220	KCS	3	50	TBD	Call TI	Call TI	-40 to 125		
TLV1117-33CDCY	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	V3	<a href="#">Samples</a>
TLV1117-33CDCYG3	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	V3	<a href="#">Samples</a>
TLV1117-33CDCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	V3	<a href="#">Samples</a>
TLV1117-33CDCYRG3	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	V3	<a href="#">Samples</a>
TLV1117-33CDRJR	ACTIVE	SON	DRJ	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 125	ZYP	<a href="#">Samples</a>
TLV1117-33CKVURG3	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	ZE33	<a href="#">Samples</a>
TLV1117-33IDCY	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	(V3 ~ VS)	<a href="#">Samples</a>
TLV1117-33IDCYG3	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	(V3 ~ VS)	<a href="#">Samples</a>



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV1117-33IDCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	VS	<a href="#">Samples</a>
TLV1117-33IDCYRG3	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	VS	<a href="#">Samples</a>
TLV1117-33IDRJR	ACTIVE	SON	DRJ	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZYR	<a href="#">Samples</a>
TLV1117-33IDRJRG4	ACTIVE	SON	DRJ	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZYR	<a href="#">Samples</a>
TLV1117-33IKVURG3	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	ZF33	<a href="#">Samples</a>
TLV1117-50CDCY	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	VT	<a href="#">Samples</a>
TLV1117-50CDCYG3	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	VT	<a href="#">Samples</a>
TLV1117-50CDCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	VT	<a href="#">Samples</a>
TLV1117-50CDCYRG3	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	VT	<a href="#">Samples</a>
TLV1117-50CDRJR	ACTIVE	SON	DRJ	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 125	ZE50	<a href="#">Samples</a>
TLV1117-50CDRJRG4	ACTIVE	SON	DRJ	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 125	ZE50	<a href="#">Samples</a>
TLV1117-50CKVURG3	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	ZE50	<a href="#">Samples</a>
TLV1117-50IDCY	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	VU	<a href="#">Samples</a>
TLV1117-50IDCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	VU	<a href="#">Samples</a>
TLV1117-50IDCYRG3	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	VU	<a href="#">Samples</a>
TLV1117-50IDRJR	ACTIVE	SON	DRJ	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZF50	<a href="#">Samples</a>
TLV1117-50IDRJRG4	ACTIVE	SON	DRJ	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZF50	<a href="#">Samples</a>
TLV1117-50IKVURG3	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	ZF50	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV1117CDCY	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	V4	<a href="#">Samples</a>
TLV1117CDCYG3	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	V4	<a href="#">Samples</a>
TLV1117CDCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	V4	<a href="#">Samples</a>
TLV1117CDCYRG3	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	V4	<a href="#">Samples</a>
TLV1117CDRJR	ACTIVE	SON	DRJ	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 125	ZYS	<a href="#">Samples</a>
TLV1117CKCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	TLV1117C	<a href="#">Samples</a>
TLV1117CKCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	TLV1117C	<a href="#">Samples</a>
TLV1117CKCT	ACTIVE	TO-220	KCT	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	TLV1117C	<a href="#">Samples</a>
TLV1117CKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	TLV1117C	<a href="#">Samples</a>
TLV1117CKTTRG3	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	TLV1117C	<a href="#">Samples</a>
TLV1117CKVURG3	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	TV1117	<a href="#">Samples</a>
TLV1117IDCY	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	V2	<a href="#">Samples</a>
TLV1117IDCYG3	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	V2	<a href="#">Samples</a>
TLV1117IDCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	V2	<a href="#">Samples</a>
TLV1117IDCYRG3	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	V2	<a href="#">Samples</a>
TLV1117IDRJR	ACTIVE	SON	DRJ	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZYT	<a href="#">Samples</a>
TLV1117IKCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 125	TLV1117I	<a href="#">Samples</a>
TLV1117IKCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 125	TLV1117I	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV1117IKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TLV1117I	<a href="#">Samples</a>
TLV1117IKTTRG3	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TLV1117I	<a href="#">Samples</a>
TLV1117IKVURG3	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	TY1117	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1117-15CDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-15CDRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117-15IDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-15IDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.0	7.42	2.0	8.0	12.0	Q3
TLV1117-15IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.8	8.0	16.0	Q2
TLV1117-15IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117-18CDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	1.5	12.0	Q3
TLV1117-18CDRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117-18CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117-18CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.8	8.0	16.0	Q2
TLV1117-18IDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.0	7.42	2.0	8.0	12.0	Q3
TLV1117-18IDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	1.5	12.0	Q3
TLV1117-18IDRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117-18IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.8	8.0	16.0	Q2
TLV1117-18IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117-25CDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-25CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.8	8.0	16.0	Q2
TLV1117-25CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1117-25IDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-25IDRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117-33CDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-33CDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.0	7.42	2.0	8.0	12.0	Q3
TLV1117-33CDRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117-33CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.8	8.0	16.0	Q2
TLV1117-33CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117-33IDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-33IDRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117-33IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.8	8.0	16.0	Q2
TLV1117-33IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117-50CDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-50CDRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117-50CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117-50CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.8	8.0	16.0	Q2
TLV1117-50IDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-50IDRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117-50IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117-50IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.8	8.0	16.0	Q2
TLV1117CDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	1.5	12.0	Q3
TLV1117CDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.0	7.42	2.0	8.0	12.0	Q3
TLV1117CDRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117CKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
TLV1117CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.8	8.0	16.0	Q2
TLV1117CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117IDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	1.5	12.0	Q3
TLV1117IDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.0	7.42	2.0	8.0	12.0	Q3
TLV1117IDRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117IKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.1	4.9	16.0	24.0	Q2
TLV1117IKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
TLV1117IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.8	8.0	16.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

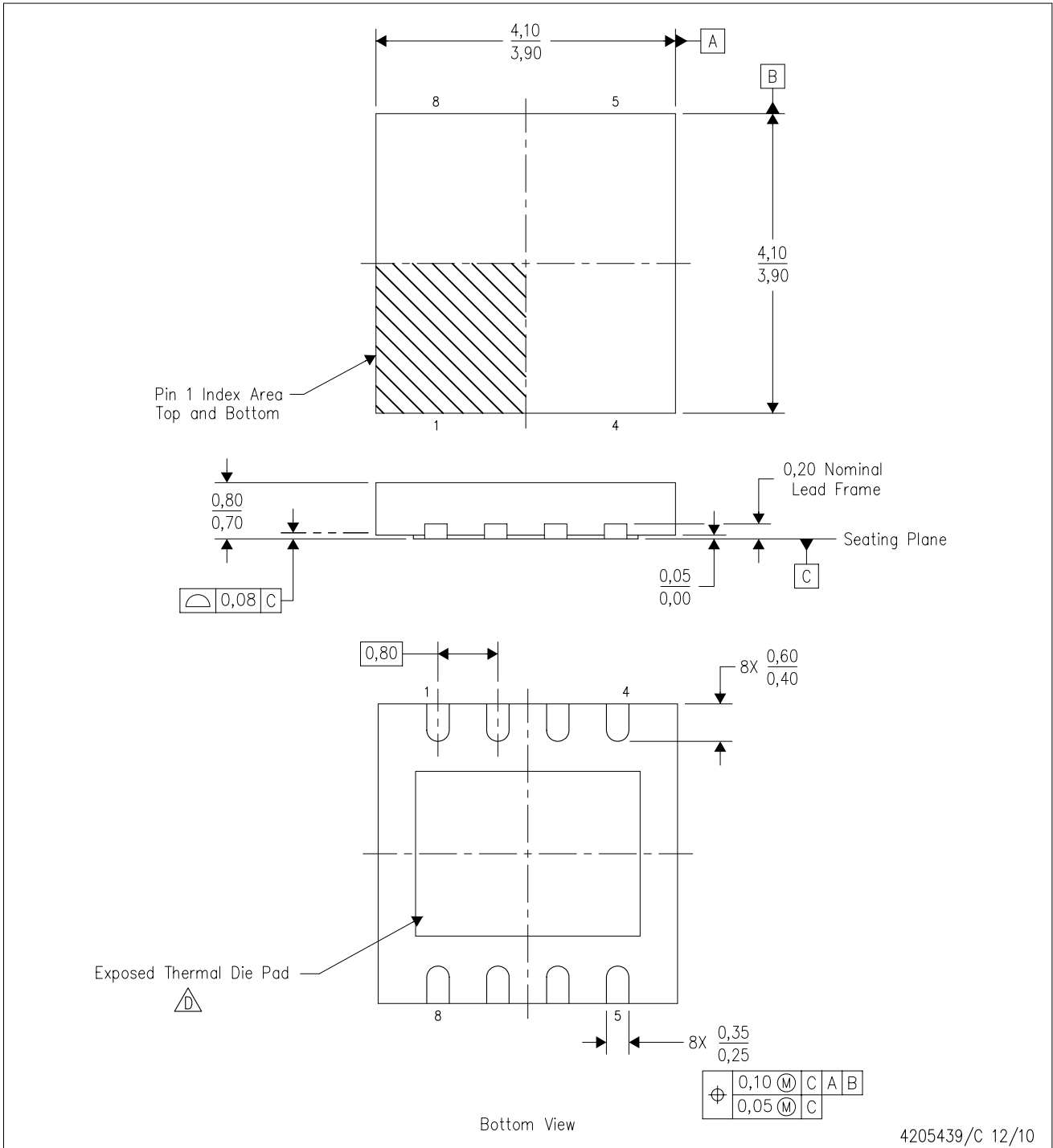
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1117-15CDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-15CDRJR	SON	DRJ	8	1000	210.0	185.0	35.0
TLV1117-15IDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-15IDCYR	SOT-223	DCY	4	2500	350.0	334.0	47.0
TLV1117-15IKVURG3	TO-252	KVU	3	2500	350.0	334.0	47.0
TLV1117-15IKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117-18CDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
TLV1117-18CDRJR	SON	DRJ	8	1000	210.0	185.0	35.0
TLV1117-18CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117-18CKVURG3	TO-252	KVU	3	2500	350.0	334.0	47.0
TLV1117-18IDCYR	SOT-223	DCY	4	2500	350.0	334.0	47.0
TLV1117-18IDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
TLV1117-18IDRJR	SON	DRJ	8	1000	210.0	185.0	35.0
TLV1117-18IKVURG3	TO-252	KVU	3	2500	350.0	334.0	47.0
TLV1117-18IKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117-25CDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-25CKVURG3	TO-252	KVU	3	2500	350.0	334.0	47.0
TLV1117-25CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117-25IDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-25IDRJR	SON	DRJ	8	1000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1117-33CDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-33CDCYR	SOT-223	DCY	4	2500	350.0	334.0	47.0
TLV1117-33CDRJR	SON	DRJ	8	1000	210.0	185.0	35.0
TLV1117-33CKVURG3	TO-252	KVU	3	2500	350.0	334.0	47.0
TLV1117-33CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117-33IDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-33IDRJR	SON	DRJ	8	1000	210.0	185.0	35.0
TLV1117-33IKVURG3	TO-252	KVU	3	2500	350.0	334.0	47.0
TLV1117-33IKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117-50CDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-50CDRJR	SON	DRJ	8	1000	210.0	185.0	35.0
TLV1117-50CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117-50CKVURG3	TO-252	KVU	3	2500	350.0	334.0	47.0
TLV1117-50IDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-50IDRJR	SON	DRJ	8	1000	210.0	185.0	35.0
TLV1117-50IKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117-50IKVURG3	TO-252	KVU	3	2500	350.0	334.0	47.0
TLV1117CDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
TLV1117CDCYR	SOT-223	DCY	4	2500	350.0	334.0	47.0
TLV1117CDRJR	SON	DRJ	8	1000	210.0	185.0	35.0
TLV1117CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
TLV1117CKVURG3	TO-252	KVU	3	2500	350.0	334.0	47.0
TLV1117CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117IDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
TLV1117IDCYR	SOT-223	DCY	4	2500	350.0	334.0	47.0
TLV1117IDRJR	SON	DRJ	8	1000	210.0	185.0	35.0
TLV1117IKTTR	DDPAK/TO-263	KTT	3	500	350.0	334.0	47.0
TLV1117IKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
TLV1117IKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117IKVURG3	TO-252	KVU	3	2500	350.0	334.0	47.0




DRJ (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



4205439/C 12/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. SON (Small Outline No-Lead) package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Package complies to JEDEC MO-229 variation WGGB.

## THERMAL PAD MECHANICAL DATA

DRJ (S-PWSON-N8)

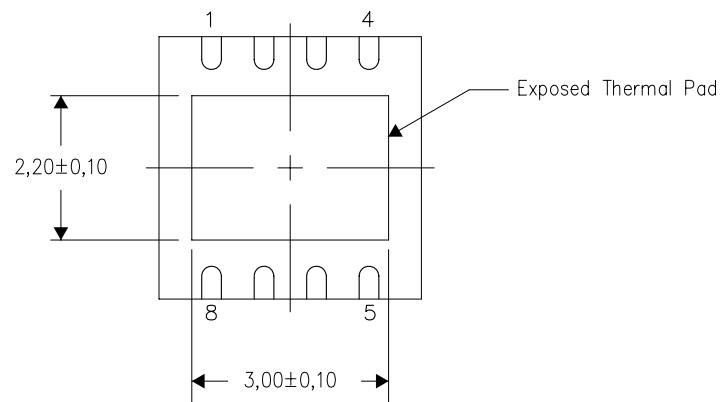
PLASTIC SMALL OUTLINE NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

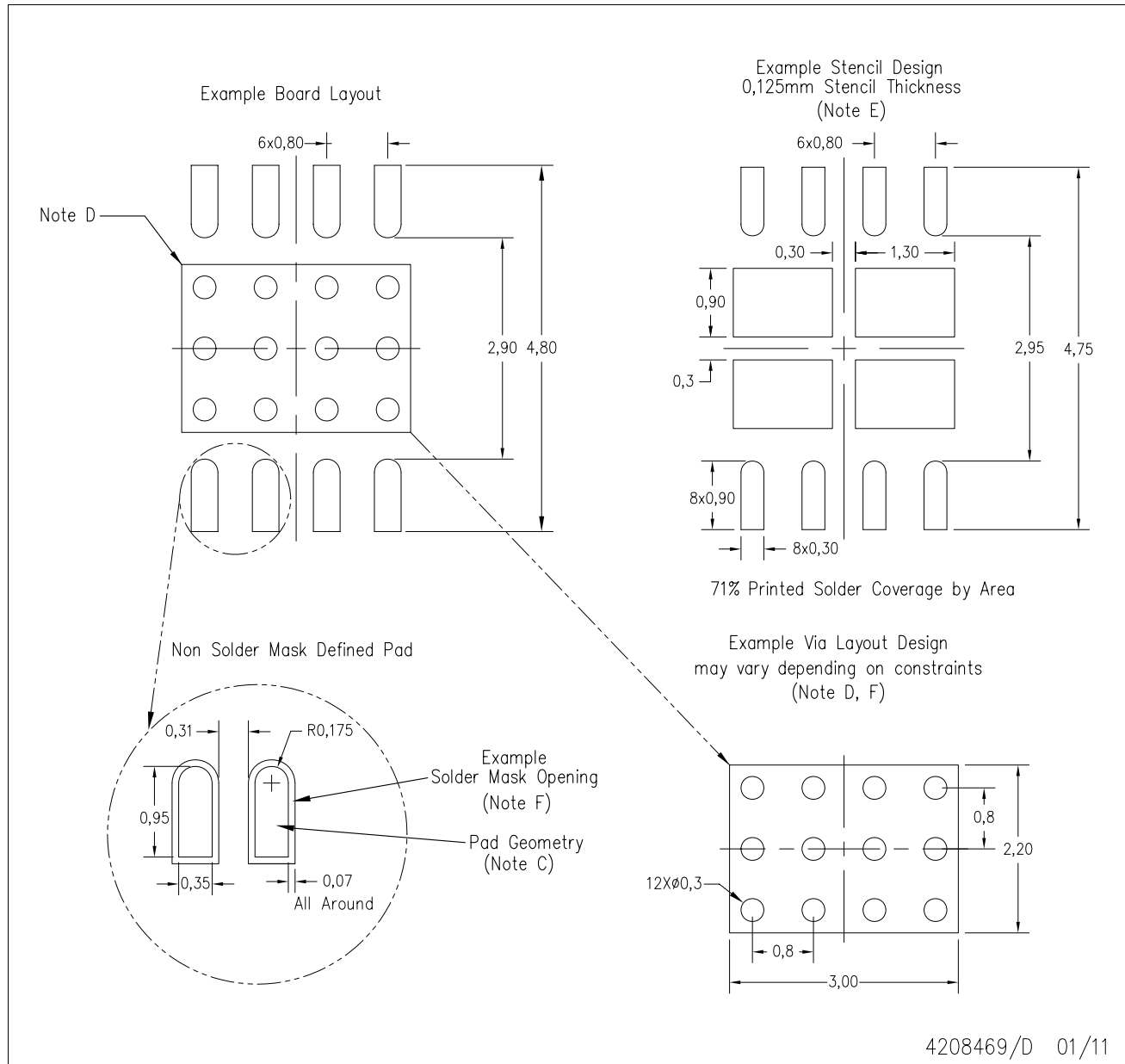
Exposed Thermal Pad Dimensions

4206882/F 01/11

NOTE: All linear dimensions are in millimeters

DRJ (S-PWSON-N8)

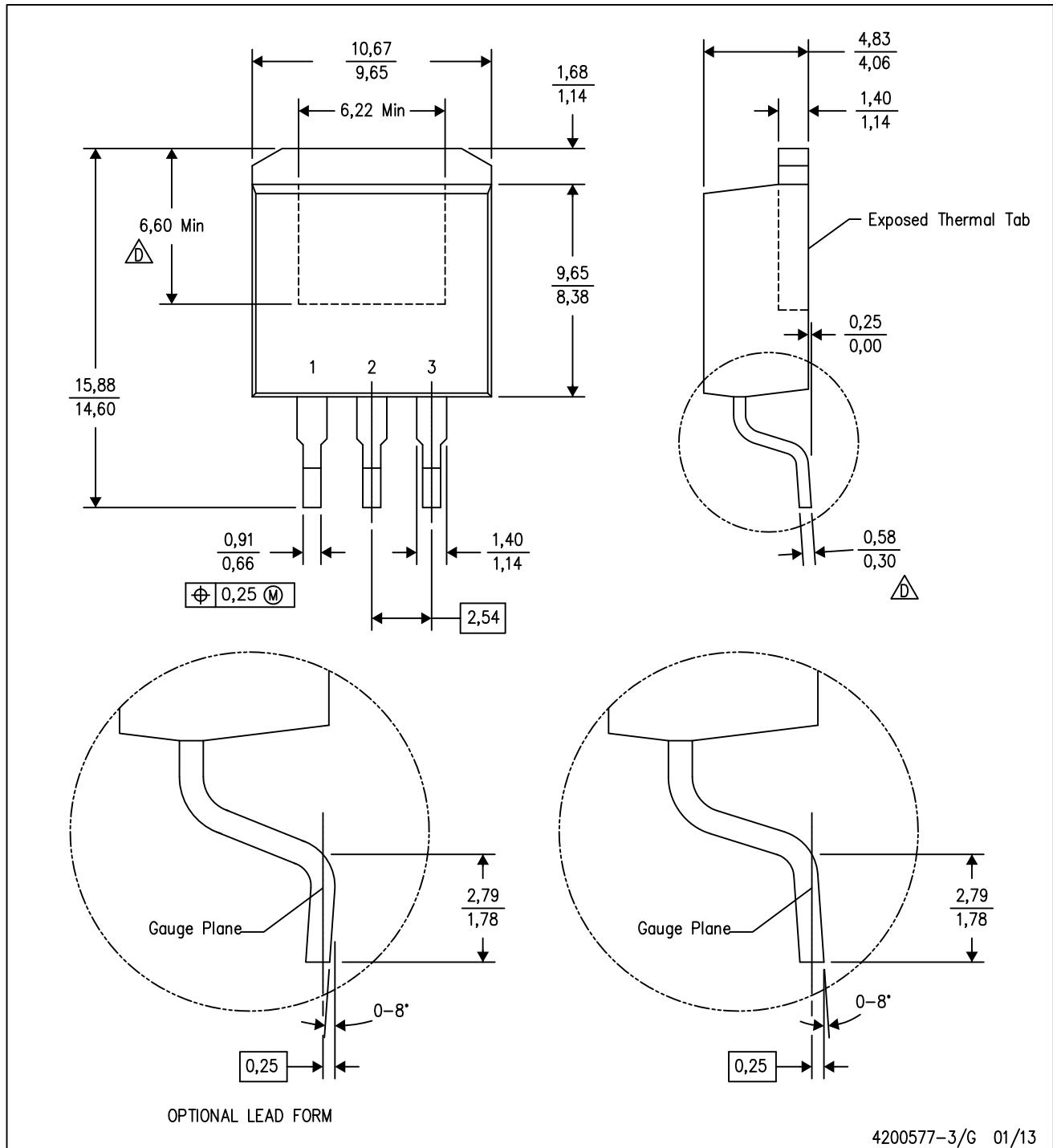
SMALL PACKAGE OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for solder mask tolerances and vias tenting recommendations for vias placed in the thermal pad.

KTT (R-PSFM-G3)

PLASTIC FLANGE-MOUNT PACKAGE

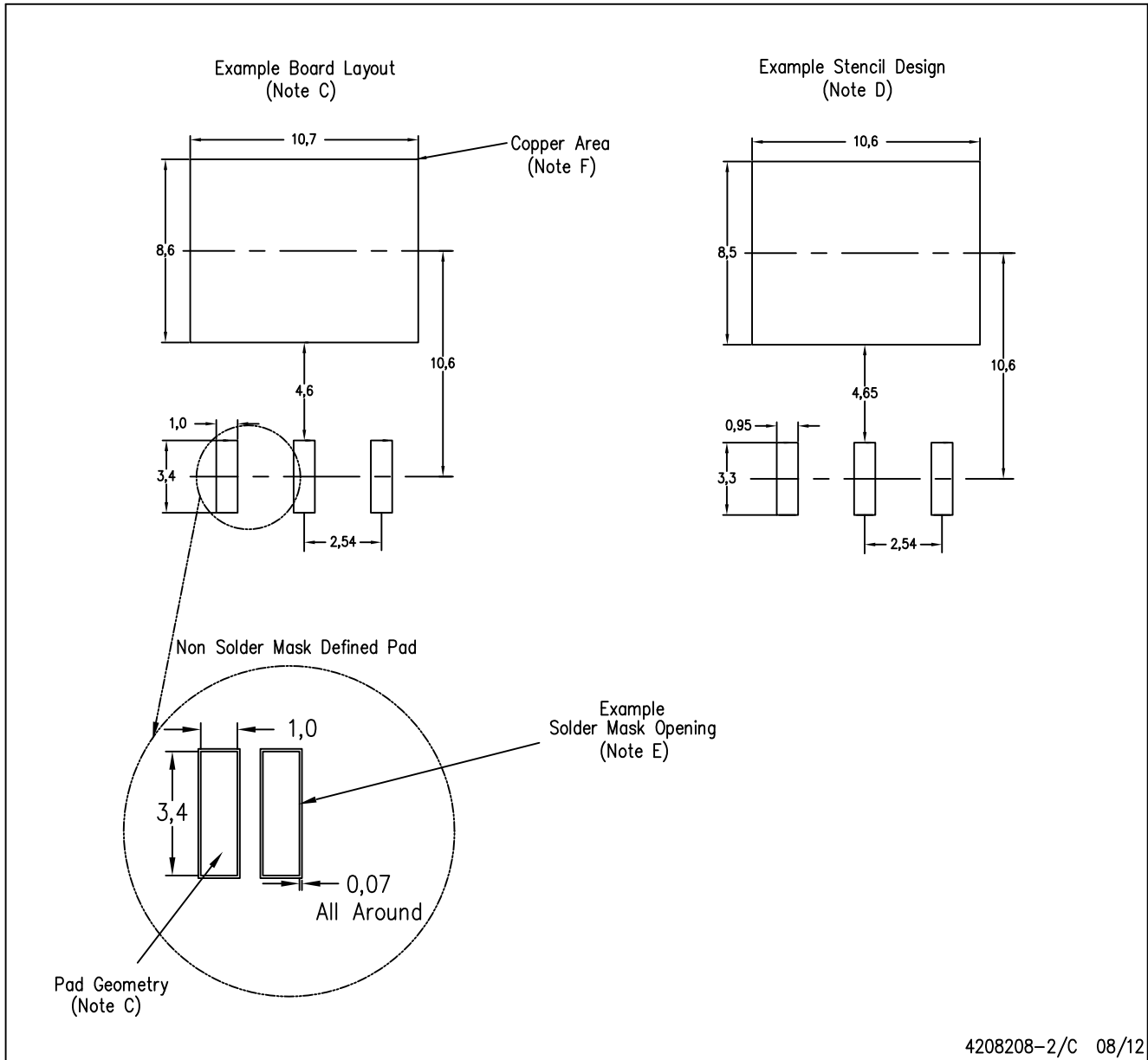


4200577-3/G 01/13

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
- Falls within JEDEC TO-263 variation AA, except minimum lead thickness and minimum exposed pad length.

KTT (R-PSFM-G3)

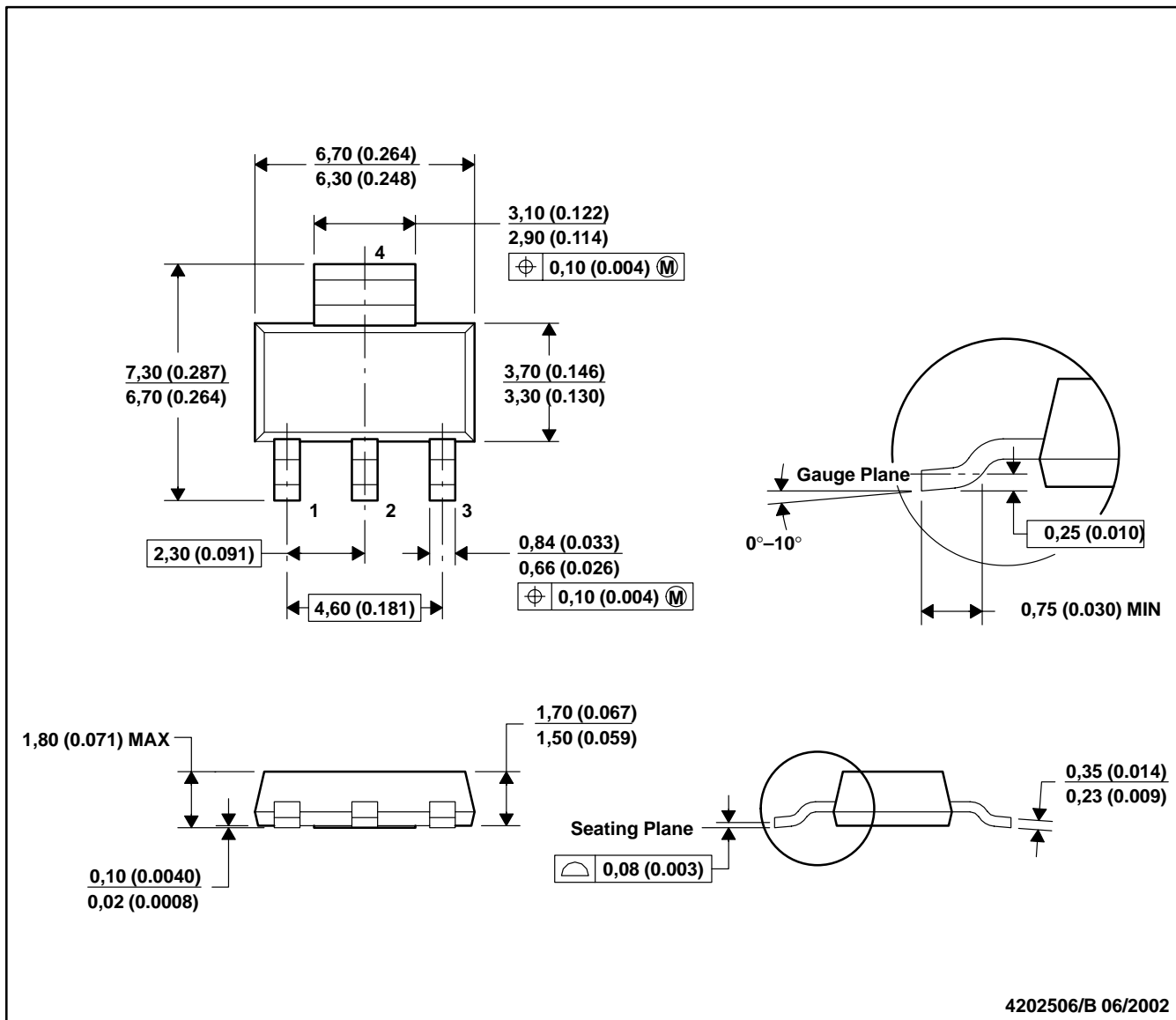
PLASTIC FLANGE-MOUNT PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-SM-782 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
  - F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

DCY (R-PDSO-G4)

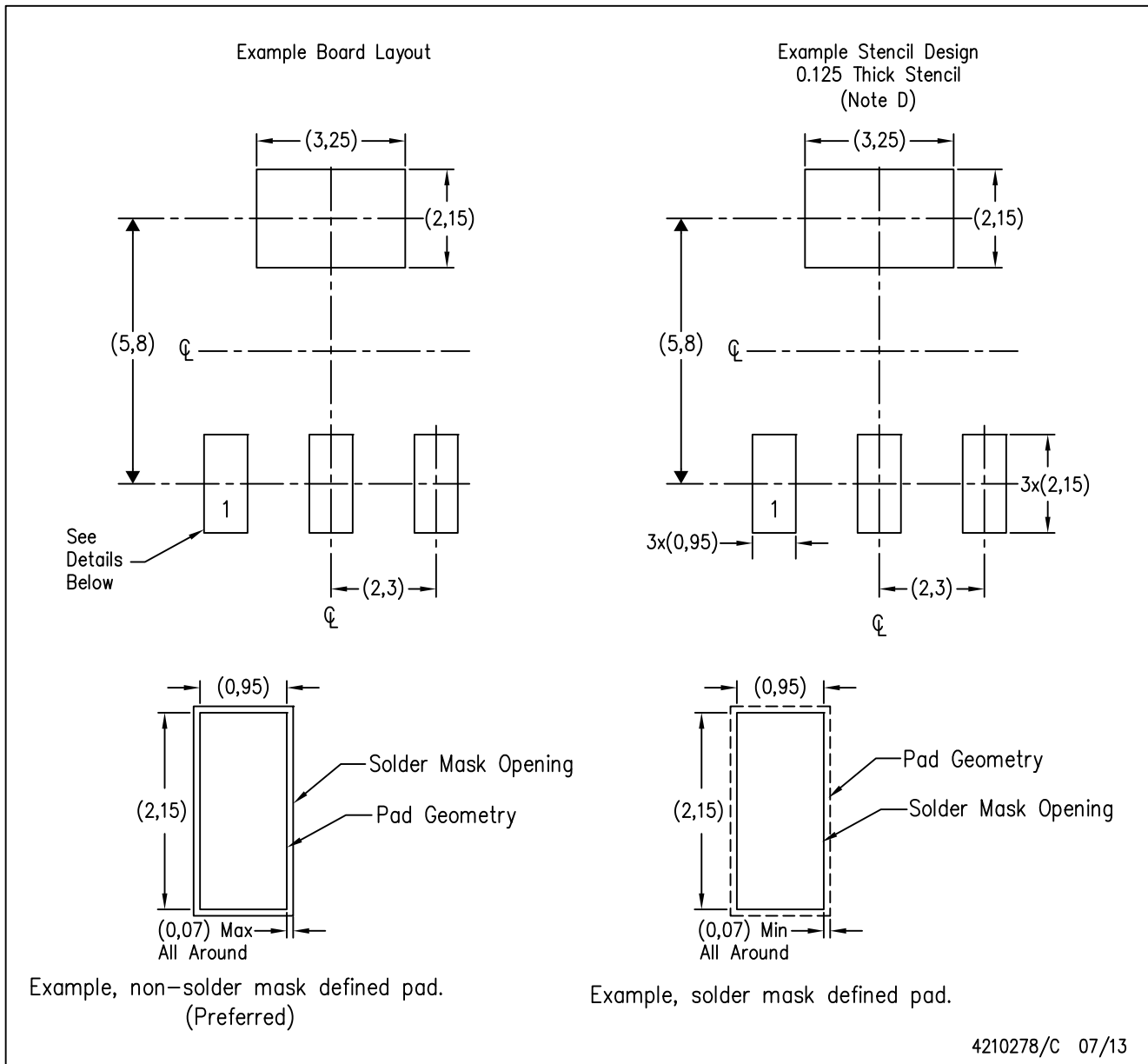
PLASTIC SMALL-OUTLINE



- NOTES: A. All linear dimensions are in millimeters (inches).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion.  
 D. Falls within JEDEC TO-261 Variation AA.

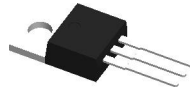
DCY (R-PDSO-G4)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil recommendations. Refer to IPC 7525 for stencil design considerations.

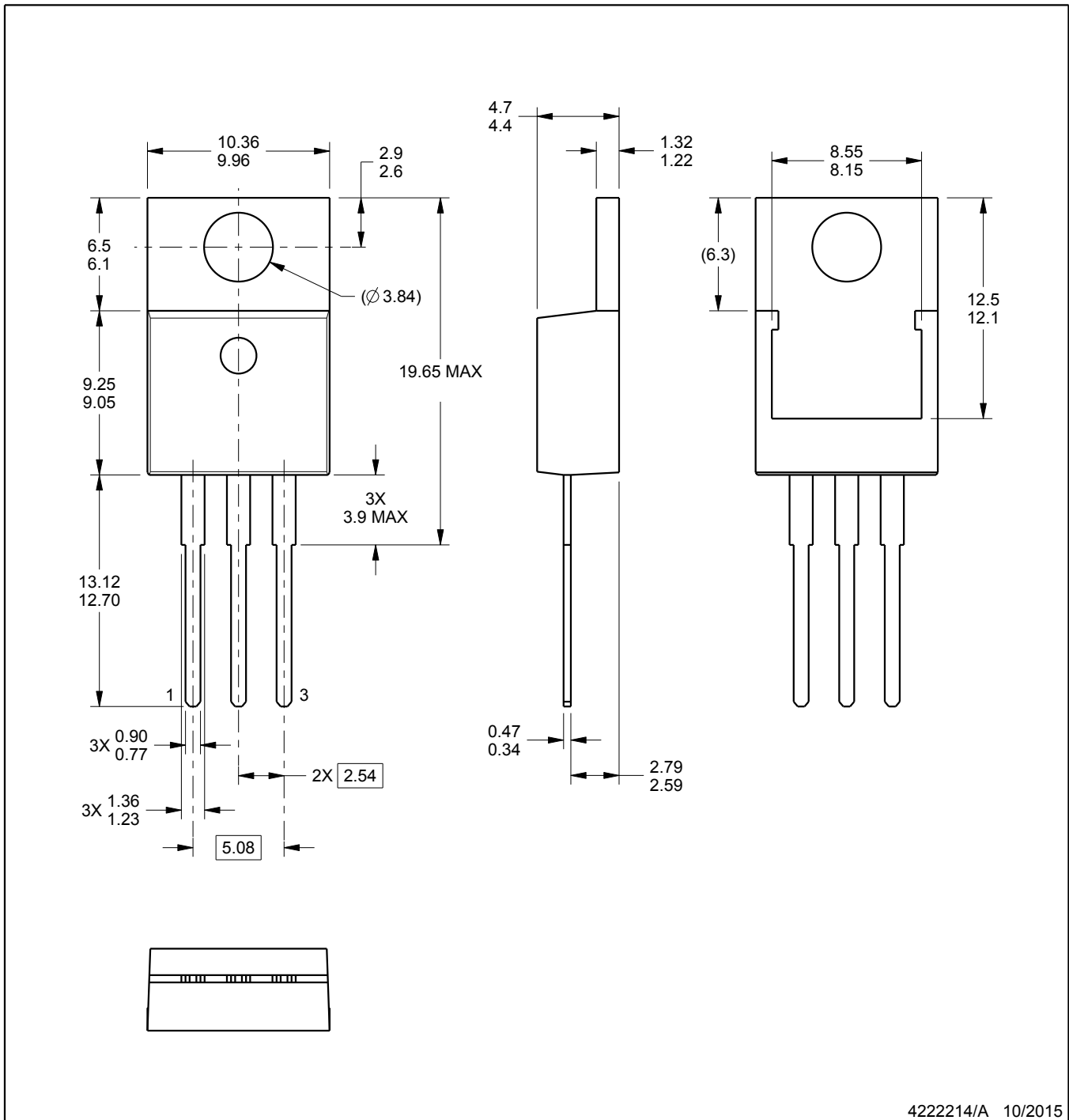
# KCS0003B



# PACKAGE OUTLINE

TO-220 - 19.65 mm max height

TO-220



4222214/A 10/2015

## NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.

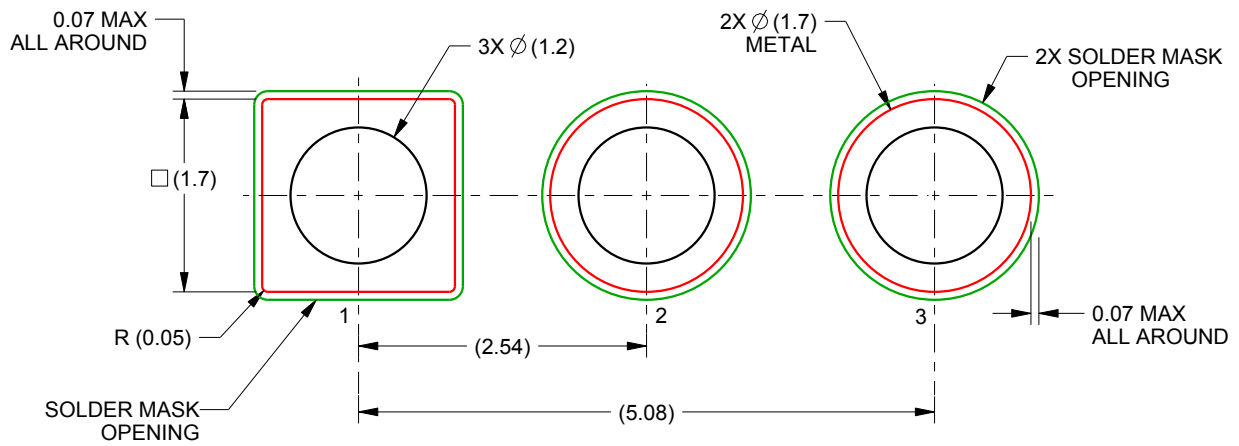


# EXAMPLE BOARD LAYOUT

KCS0003B

TO-220 - 19.65 mm max height

TO-220

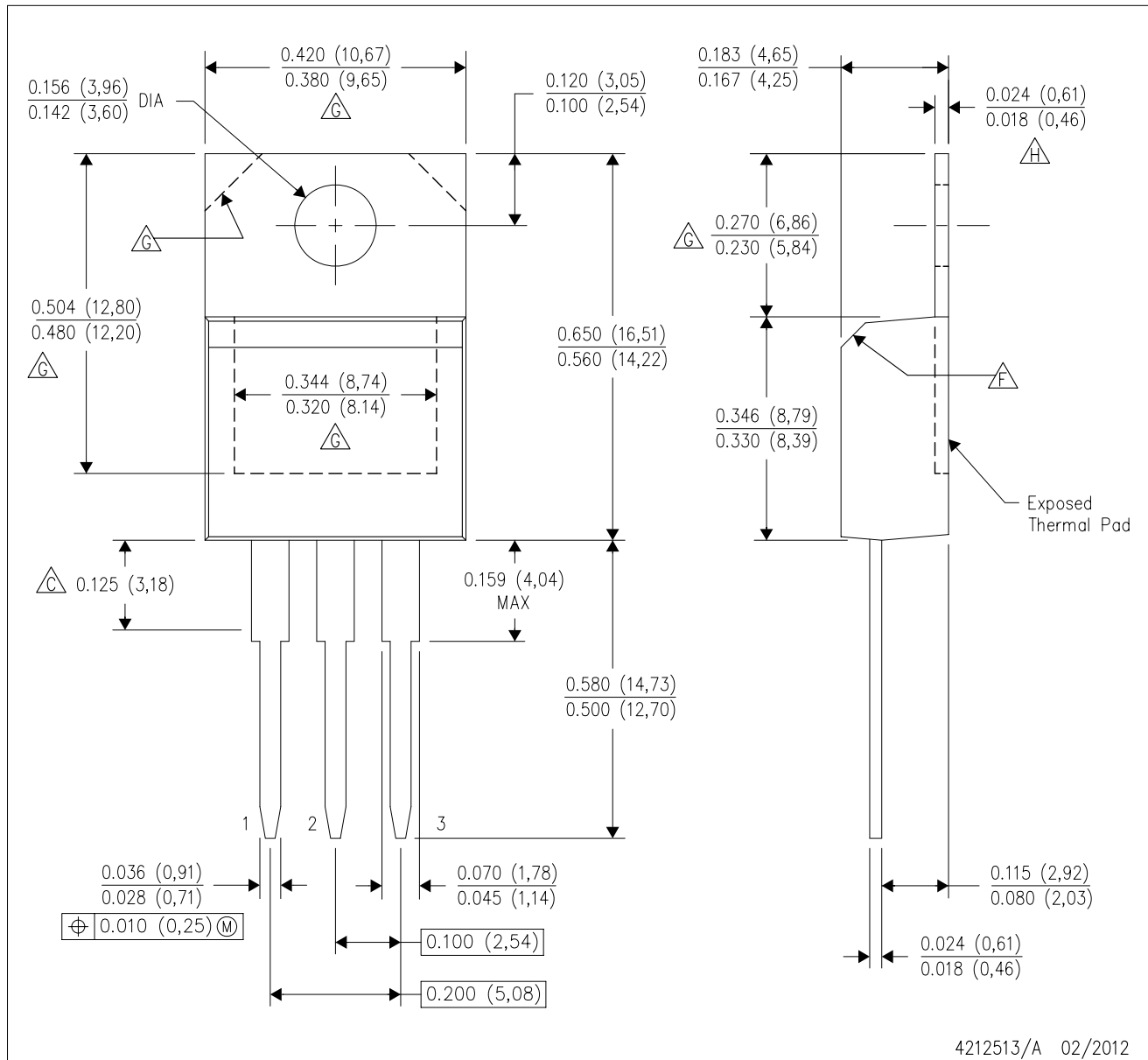


LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 15X

4222214/A 10/2015

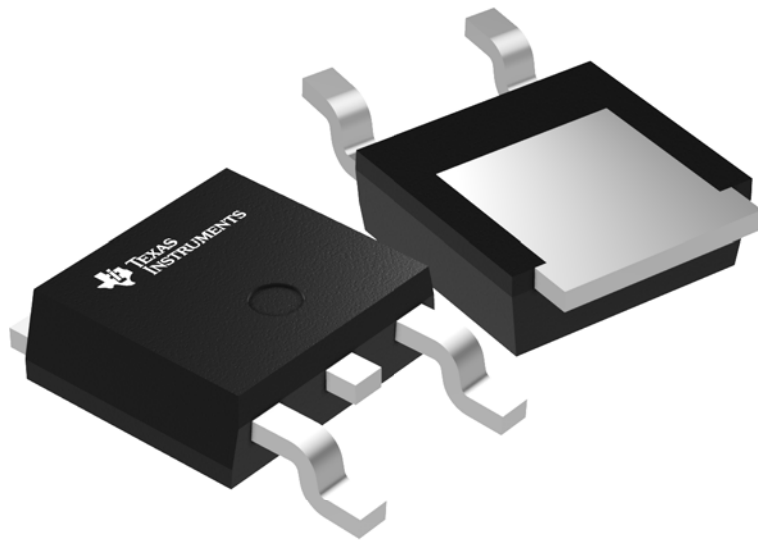
KCT (R-PSFM-T3)

PLASTIC FLANGE-MOUNT PACKAGE



4212513/A 02/2012

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Lead dimensions are not controlled within this area.
  - D. All lead dimensions apply before solder dip.
  - E. The center lead is in electrical contact with the mounting tab.
  - F. The chamfer is optional.
  - G. Thermal pad contour optional within these dimensions.
  - H. Falls within JEDEC TO-220 variation AB, except minimum tab thickness.



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



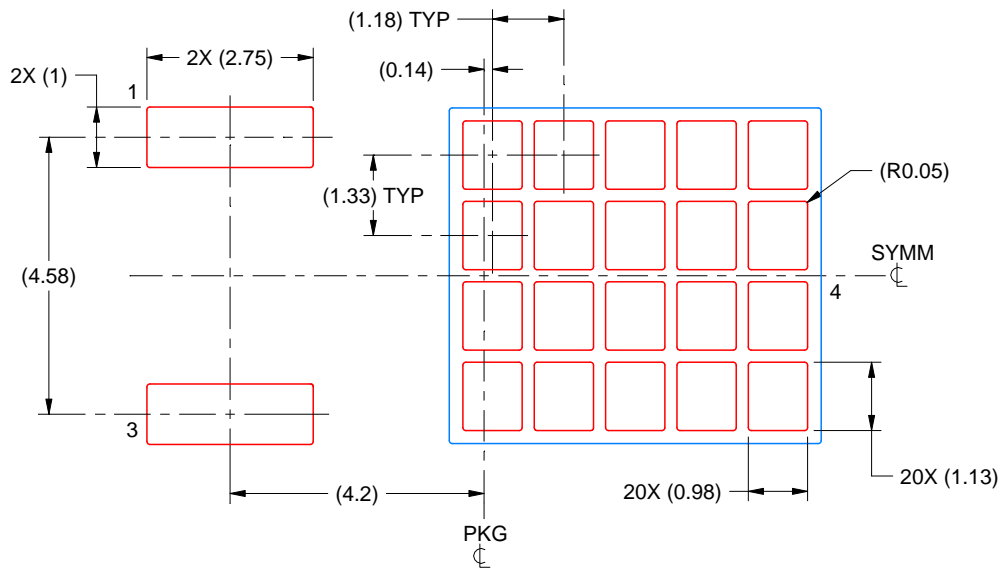


# EXAMPLE STENCIL DESIGN

KVU0003A

TO-252 - 2.52 mm max height

TO-252



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
65% PRINTED SOLDER COVERAGE BY AREA  
SCALE:8X

4218915/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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