

## 20A, 500V N-CHANNEL MOSFET

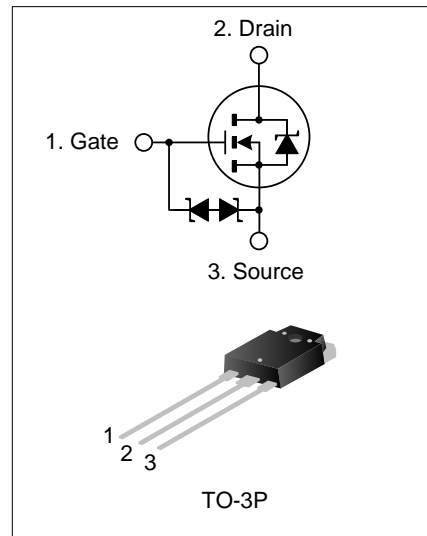
### DESCRIPTION

SVF20NE50PN is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

### FEATURES

- \* 20A, 500V,  $R_{DS(on)}(typ.)=0.18\Omega@V_{GS}=10V$
- \* Low gate charge
- \* Low Crss
- \* Fast switching
- \* Improved dv/dt capability



### ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SVF20NE50PN	TO-3P	20NE50	Pb free	Tube

**ABSOLUTE MAXIMUM RATINGS** (unless otherwise noted,  $T_C=25^{\circ}\text{C}$ )

Characteristics	Symbol	Ratings	Unit
Drain-Source Voltage	$V_{DS}$	500	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	V
Drain Current	$I_D$	$T_C=25^{\circ}\text{C}$	20.0
		$T_C=100^{\circ}\text{C}$	12.6
Drain Current Pulsed	$I_{DM}$	80.0	A
Power Dissipation ( $T_C=25^{\circ}\text{C}$ ) -Derate above $25^{\circ}\text{C}$	$P_D$	252	W
		2.02	W/ $^{\circ}\text{C}$
Single Pulsed Avalanche Energy (Note 1)	$E_{AS}$	2812	mJ
Operation Junction Temperature Range	$T_J$	$-55\sim+150$	$^{\circ}\text{C}$
Storage Temperature Range	$T_{stg}$	$-55\sim+150$	$^{\circ}\text{C}$

**THERMAL CHARACTERISTICS**

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.50	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	$^{\circ}\text{C}/\text{W}$

**ELECTRICAL CHARACTERISTICS** (unless otherwise noted,  $T_C=25^{\circ}\text{C}$ )

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	$B_{VDSS}$	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	500	--	--	V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=500\text{V}, V_{GS}=0\text{V}$	--	--	1.0	$\mu\text{A}$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 25\text{V}, V_{DS}=0\text{V}$	--	--	$\pm 100$	$\mu\text{A}$
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu\text{A}$	2.0	--	4.0	V
On State Resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=10.0\text{A}$	--	0.18	0.27	$\Omega$
Input Capacitance	$C_{iss}$	$V_{DS}=25\text{V}, V_{GS}=0\text{V},$ $f=1.0\text{MHZ}$	--	3504.0	--	pF
Output Capacitance	$C_{oss}$		--	425.0	--	
Reverse Transfer Capacitance	$C_{rss}$		--	12.03	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=250\text{V}, R_G=25\Omega,$ $I_D=20.0\text{A}$  (Note2,3)	--	80.67	--	ns
Turn-on Rise Time	$t_r$		--	150.67	--	
Turn-off Delay Time	$t_{d(off)}$		--	198.67	--	
Turn-off Fall Time	$t_f$		--	112.0	--	
Total Gate Charge	$Q_g$	$V_{DD}=400\text{V}, V_{GS}=10\text{V},$ $I_D=20.0\text{A}$  (Note 2, 3)	--	58.38	--	nC
Gate-Source Charge	$Q_{gs}$		--	16.89	--	
Gate-Drain Charge	$Q_{gd}$		--	18.33	--	

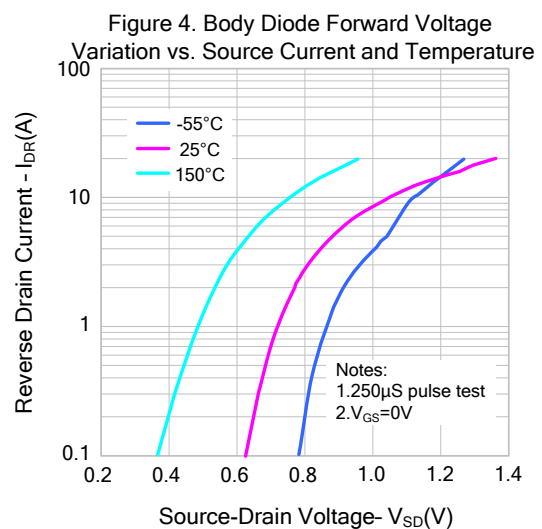
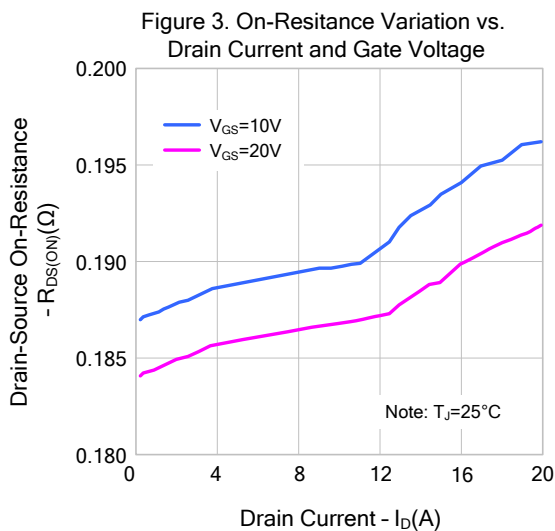
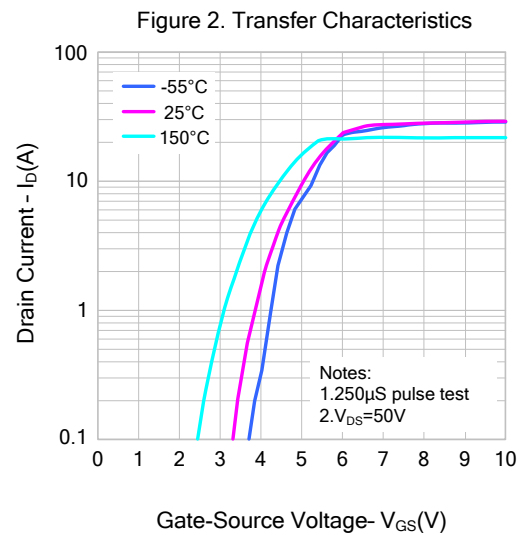
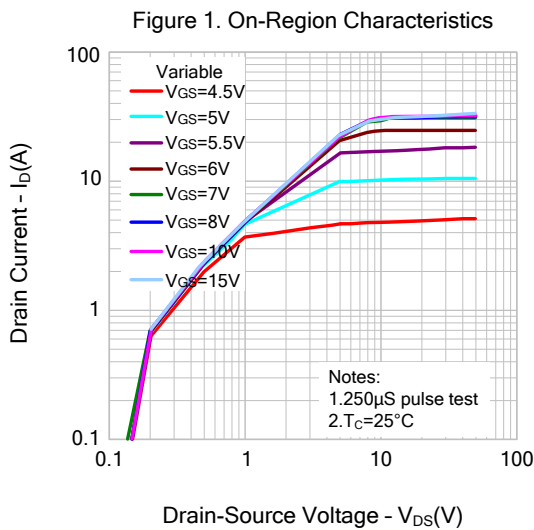
**SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS**

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Source Current	$I_S$	Integral Reverse P-N	--	--	20.0	A
Pulsed Source Current	$I_{SM}$	Junction Diode in the MOSFET	--	--	80.0	
Diode Forward Voltage	$V_{SD}$	$I_S=20.0A, V_{GS}=0V$	--	--	1.3	V
Reverse Recovery Time	$T_{rr}$	$I_S=20.0A, V_{GS}=0V,$	--	577.53	--	ns
Reverse Recovery Charge	$Q_{rr}$	$di/dt=100A/\mu S$ (Note2)	--	7.78	--	$\mu C$

**Notes:**

1.  $L=30mH, I_{AS}=11.60A, V_{DD}=165V, R_G=25\Omega,$  starting  $T_J=25^\circ C$ ;
2. Pulse Test: Pulse width  $\leq 300\mu s,$  Duty cycles  $\leq 2\%$ ;
3. Essentially independent of operating temperature.

**TYPICAL CHARACTERISTICS**





TYPICAL CHARACTERISTICS

Figure 5. Capacitance Characteristics

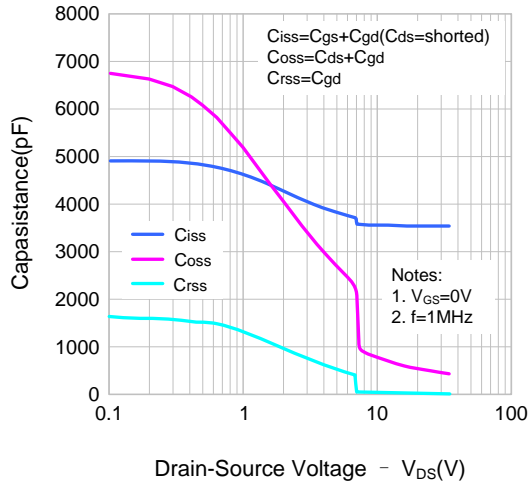


Figure 6. Gate Charge Characteristics

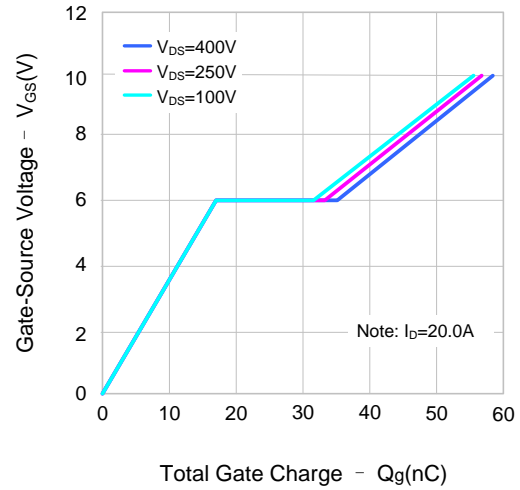


Figure 7. Breakdown Voltage Variation vs. Temperature

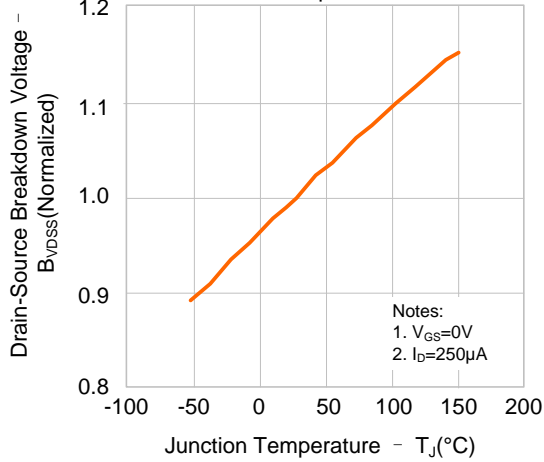


Figure 8. On-resistance Variation vs. Temperature

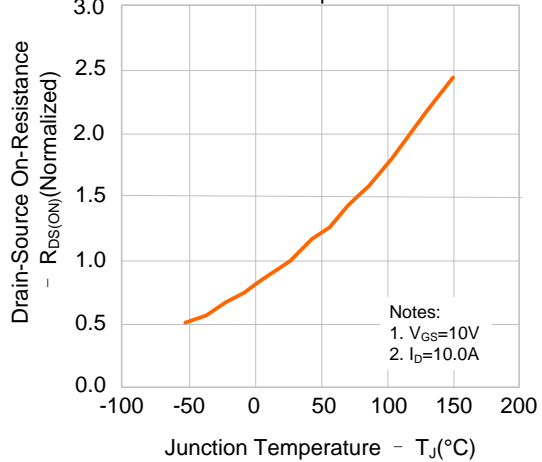


Figure 9. Max. Safe Operating Area

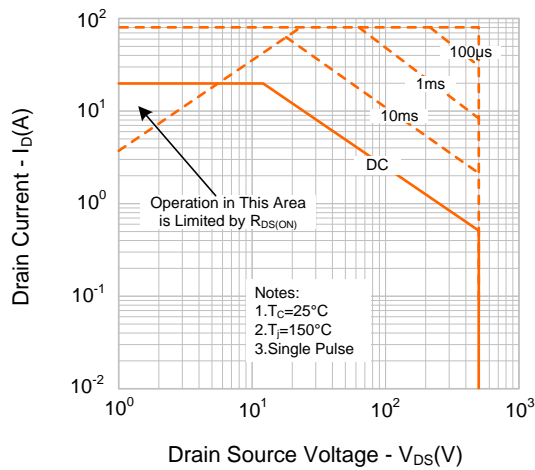
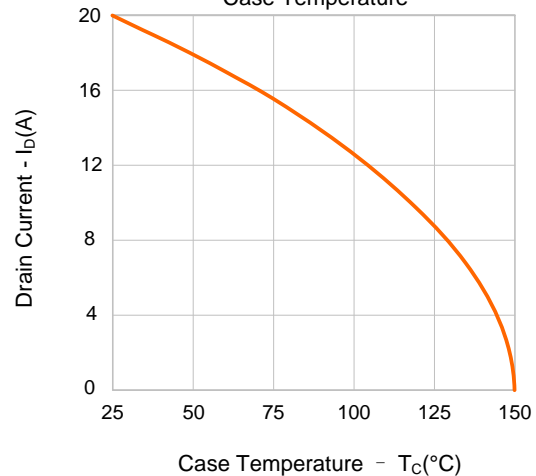
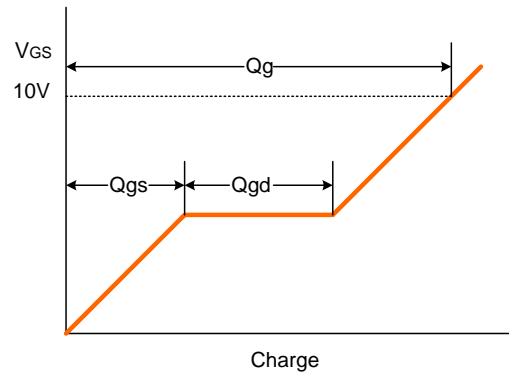
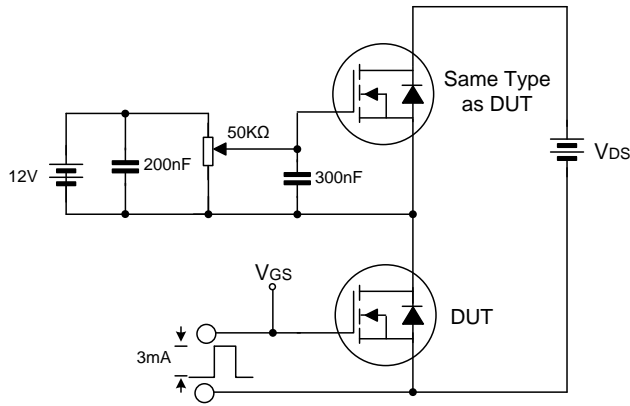


Figure 10. Maximum Drain Current vs. Case Temperature

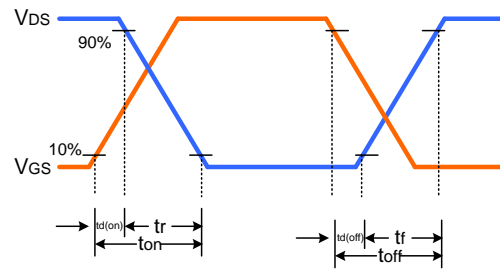
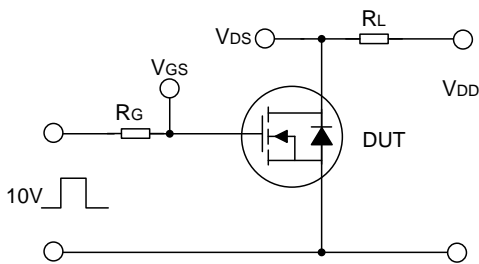


**TYPICAL TEST CIRCUIT**

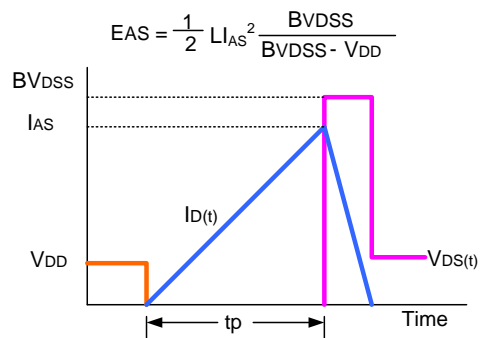
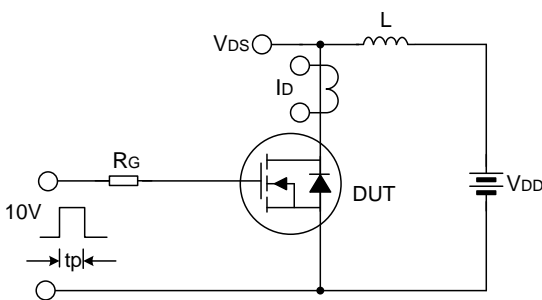
Gate Charge Test Circuit & Waveform



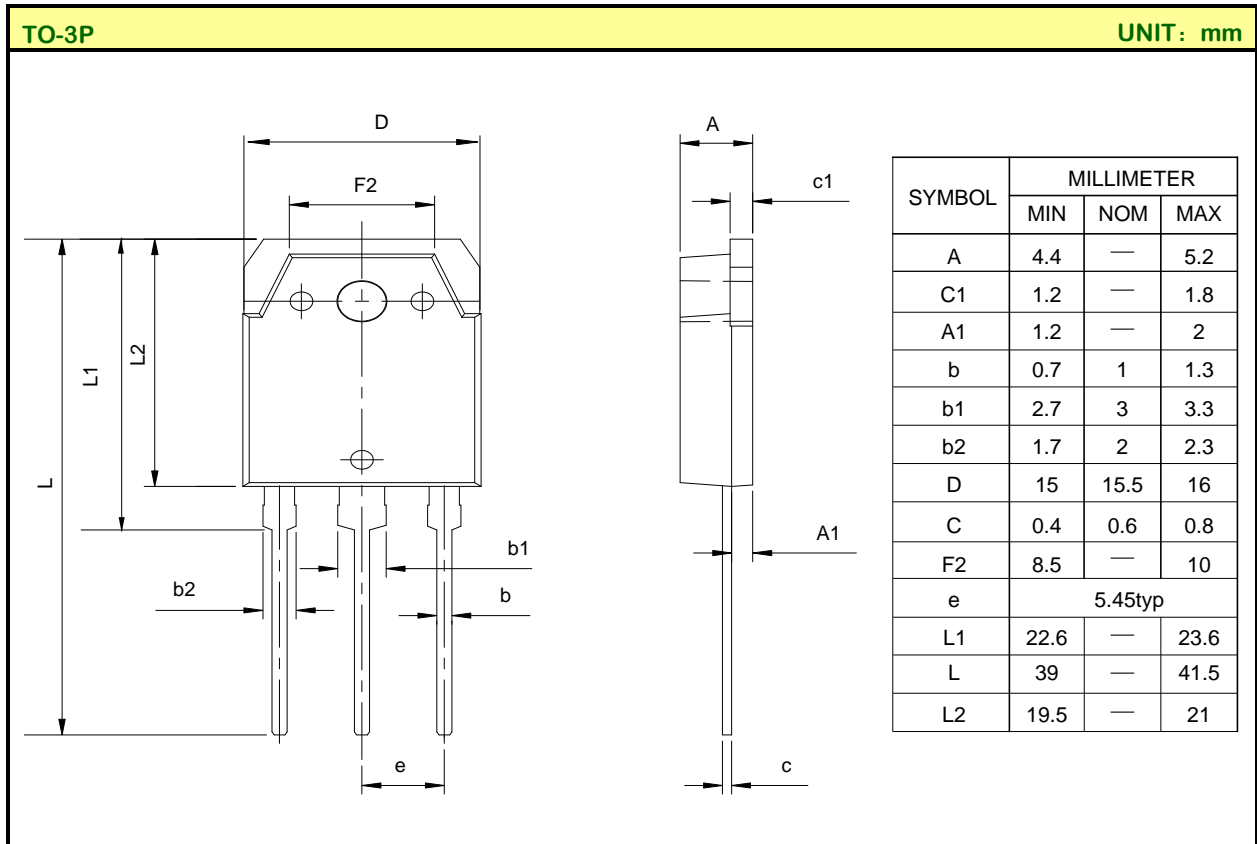
Switching Test Circuit & Waveform



EAS Test Circuit & Waveform



**PACKAGE OUTLINE**



**Disclaimer:**

- Silan reserves the right to make changes to the information herein for the improvement of the design and performance without further notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.
- All semiconductor products malfunction or fail with some probability under special conditions. When using Silan products in system design or complete machine manufacturing, it is the responsibility of the buyer to comply with the safety standards strictly and take essential measures to avoid situations in which a malfunction or failure of such Silan products could cause loss of body injury or damage to property.
- Silan will supply the best possible product for customers!



## ATTACHMENT

### Revision History

Date	REV	Description	Page
2011.05.17	1.0	Initial release	
2012.06.04	1.1	Modify the values of $T_{rr}$ and $Q_{rr}$	
2013.07.23	1.2	Modify "TYPICAL CHARACTERISTICS"	
2020.06.10	1.3	Delete NOMENCLATURE	