

SN54AC373, SN74AC373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SCAS540D – OCTOBER 1995 – REVISED OCTOBER 2003

- 2-V to 6-V V_{CC} Operation
- Inputs Accept Voltages to 6 V
- Max t_{pd} of 9.5 ns at 5 V
- 3-State Noninverting Outputs Drive Bus Lines Directly
- Full Parallel Access for Loading

description/ordering information

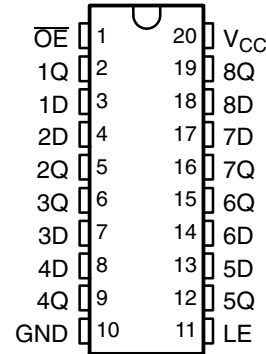
These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are D-type transparent latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

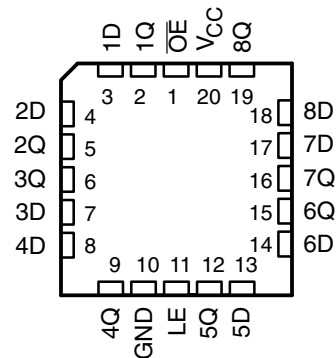
A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines in bus-organized systems without need for interface or pullup components.

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

SN54AC373 . . . J OR W PACKAGE
SN74AC373 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AC373 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74AC373N	SN74AC373N
	SOIC – DW	Tube	SN74AC373DW	AC373
		Tape and reel	SN74AC373DWR	
	SOP – NS	Tape and reel	SN74AC373NSR	AC373
	SSOP – DB	Tape and reel	SN74AC373DBR	AC373
	TSSOP – PW	Tube	SN74AC373PW	AC373
Tape and reel		SN74AC373PWR		
-55°C to 125°C	CDIP – J	Tube	SNJ54AC373J	SNJ54AC373J
	CFP – W	Tube	SNJ54AC373W	SNJ54AC373W
	LCCC – FK	Tube	SNJ54AC373FK	SNJ54AC373FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
INSTRUMENTS**

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recommended operating conditions (see Note 3)

		SN54AC373		SN74AC373		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	6	2	6	V
V _{IH}	High-level input voltage	V _{CC} = 3 V		2.1		V
		V _{CC} = 4.5 V		3.15		
		V _{CC} = 5.5 V		3.85		
V _{IL}	Low-level input voltage	V _{CC} = 3 V		0.9		V
		V _{CC} = 4.5 V		1.35		
		V _{CC} = 5.5 V		1.65		
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 3 V		-12		mA
		V _{CC} = 4.5 V		-24		
		V _{CC} = 5.5 V		-24		
I _{OL}	Low-level output current	V _{CC} = 3 V		12		mA
		V _{CC} = 4.5 V		24		
		V _{CC} = 5.5 V		24		
Δt/Δv	Input transition rise or fall rate	8		8		ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AC373		SN74AC373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -12 mA	3 V	2.56			2.4		2.46		
		4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
V _{OL}	I _{OL} = 50 μA	3 V	0.1			0.1		0.1		V
		4.5 V	0.1			0.1		0.1		
		5.5 V	0.1			0.1		0.1		
	I _{OL} = 12 mA	3 V	0.36			0.5		0.44		
		4.5 V	0.36			0.5		0.44		
		5.5 V	0.36			0.5		0.44		
I _I	V _I = V _{CC} or GND	5.5 V	±0.1			±1		±1		μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V	±0.25			±5		±2.5		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	4			80		40		μA
C _i	V _I = V _{CC} or GND	5 V	4.5							pF



SN54AC373, SN74AC373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3 V \pm 0.3 V$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ C$		SN54AC373		SN74AC373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	5.5		6.5		6		ns
t_{su}	Setup time, data before LE↓	5.5		6.5		6		ns
t_h	Hold time, data after LE↓	1		1		1		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5 V \pm 0.5 V$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ C$		SN54AC373		SN74AC373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	4		5		4.5		ns
t_{su}	Setup time, data before LE↓	4		5		4.5		ns
t_h	Hold time, data after LE↓	1		1		1		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3 V \pm 0.3 V$ (unless otherwise noted) (see Figure 1)

PARAMETER	TO (INPUT)	TO (OUTPUT)	$T_A = 25^\circ C$			SN54AC373		SN74AC373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.5	10	13.5	1	16.5	1.5	15	ns
t_{PHL}			1.5	9.5	13.0	1	16	1.5	14.5	
t_{PLH}	LE	Q	1.5	10	13.5	1	16.5	1.5	15	ns
t_{PHL}			1.5	9.5	12.5	1	15	1.5	14	
t_{PZH}	\overline{OE}	Q	1.5	9	11.5	1	14	1	13	ns
t_{PZL}			1.5	8.5	11.5	1	13.5	1	13	
t_{PHZ}	\overline{OE}	Q	1.5	10	12.5	1	16	1	14.5	ns
t_{PLZ}			1.5	8	11.5	1	13	1	12.5	

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5 V \pm 0.5 V$ (unless otherwise noted) (see Figure 1)

PARAMETER	TO (INPUT)	TO (OUTPUT)	$T_A = 25^\circ C$			SN54AC373		SN74AC373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.5	7	9.5	1	11.5	1.5	10.5	ns
t_{PHL}			1.5	7	9.5	1	11.5	1.5	10.5	
t_{PLH}	LE	Q	1.5	7.5	9.5	1	12	1.5	10.5	ns
t_{PHL}			1.5	7	9.5	1	11	1.5	10.5	
t_{PZH}	\overline{OE}	Q	1.5	7	8.5	1	10.5	1	9.5	ns
t_{PZL}			1.5	6.5	8.5	1	10	1	9.5	
t_{PHZ}	\overline{OE}	Q	1.5	8	11	1	13.5	1	12.5	ns
t_{PLZ}			1.5	6.5	8.5	1	10.5	1	10	

operating characteristics, $V_{CC} = 5 V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50 pF, f = 1 MHz$	40	pF



SN54AC373, SN74AC373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

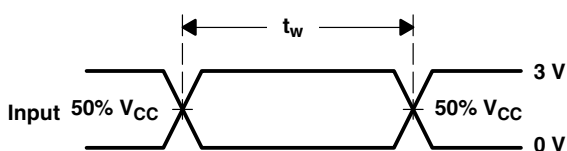
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PARAMETER MEASUREMENT INFORMATION

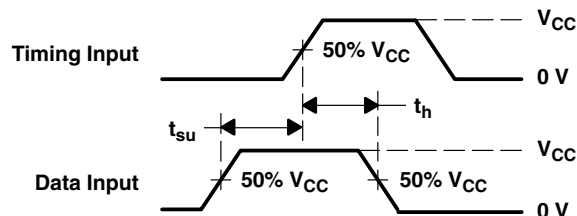


LOAD CIRCUIT

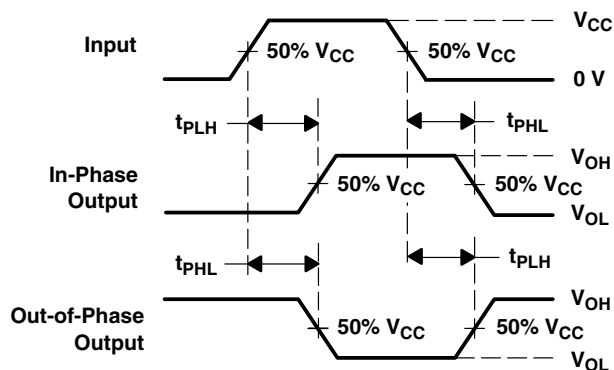
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



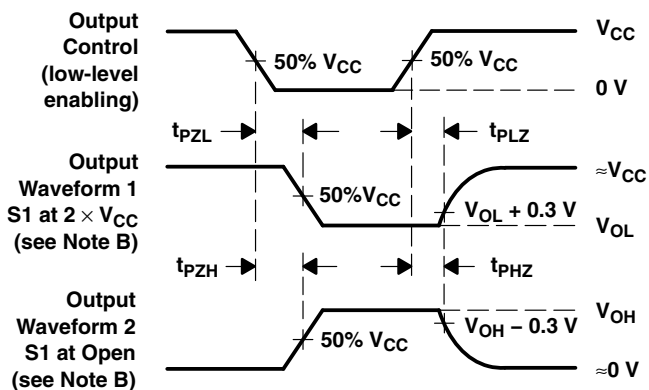
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87555012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-87555012A SNJ54AC 373FK	Samples
5962-8755501RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8755501RA SNJ54AC373J	Samples
5962-8755501SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8755501SA SNJ54AC373W	Samples
5962-8755501VSA	ACTIVE	CFP	W	20	25	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8755501VS A SNV54AC373W	Samples
SN74AC373DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC373	Samples
SN74AC373DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC373	Samples
SN74AC373DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC373	Samples
SN74AC373DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC373	Samples
SN74AC373N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AC373N	Samples
SN74AC373NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AC373N	Samples
SN74AC373NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC373	Samples
SN74AC373PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC373	Samples
SN74AC373PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC373	Samples
SNJ54AC373FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-87555012A SNJ54AC 373FK	Samples
SNJ54AC373J	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8755501RA SNJ54AC373J	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54AC373W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8755501SA SNJ54AC373W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54AC373, SN54AC373-SP, SN74AC373 :

- Catalog: [SN74AC373](#), [SN54AC373](#)

- Enhanced Product: [SN74AC373-EP](#), [SN74AC373-EP](#)
- Military: [SN54AC373](#)
- Space: [SN54AC373-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC373DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AC373DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AC373NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AC373PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC373DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74AC373DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AC373NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74AC373PWR	TSSOP	PW	20	2000	367.0	367.0	38.0

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



4040180-4/F 04/14

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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