LSI/CSI

LSI Computer Systems, Inc. 1235 Walt Whitman Road, Melville, NY 11747 (631) 271-0400 FAX (631) 271-0405

LS8290
LS8291

PRELIMINARY MICRO-STEPPING MOTOR CONTROLLER

March 2009

FEATURES:

- Controls Bipolar and Unipolar Stepper Motors
- Full,1/2, 1/4, 1/8, 1/6, 1/32, step modes selected with 2 mode inputs
- PWM chopper circuit for step and torque control
- Precision DAC reference for PWM sense comparators
- Fast / slow / mixed decay control input
- Automated switching between stepping and holding torques
- RC input for programmable current sense blanking delay
- RC input for programmable delay for switching from stepping to holding torque
- Separate reference voltages for stepping and holding torques
- Direction control input
- Reset input
- Step control input
- Enable input
- Supply current < 400uA
- 4.5V to 5.5V Operation (V_{DD} – V_{SS}).
- **LS8290** (DIP), **LS8290-S** (SOIC), **LS8290-TS** (TSSOP)
- **LS8291** (DIP), **LS8291-S** (SOIC), **LS8291-TS** (TSSOP)

– **See Figure 1 on Page 3** –

DESCRIPTION:

The **LS8290** and **LS8291** are stepper motor controllers with programmable stepping resolution from full step to 1/32 step. There are four phase-drive outputs and two inhibit outputs for controlling two-phase bipolar motors or four-phase unipolar motors. These outputs are designed to drive two external H-bridge drivers for bipolar motor windings or four external transistors for center-tapped unipolar motor windings. These controllers can also be configured to drive discrete external transistors for bipolar motor windings. A mode controlled look-up table generates the PWM duty cycles for the two motor windings corresponding to the stepping sequences. Two internal DACs convert the PWM data to analog voltages as percentages of the reference voltage applied at the VREF input. SENSE inputs are provided to monitor currents through the motor windings in terms of voltage drops across fractional-Ohm resistors in series with the H-bridge drivers. Upon turning on a PWM drive, when the SENSE voltage ramps up to the DAC output reference level, the PWM drive is switched off for the remainder of the PWM period. The PWM period is fixed at Tpwm = 256/fc, where fc is the clock frequency at CLK input. The PWM cycles for the two drives are started simultaneously but terminated at different instants to correspond to the individual DAC output references.

Input is provided for a power saving holding-torque mode at a lower current when the motor is not turning. The holding torque level is selected by a separate voltage reference applied at the VREFH input. This reference voltage is automatically switched in at the end of a programmable delay following a micro-step.

PWM chopping can be controlled by either chopping the INHIBIT outputs or the PHASE outputs. The chopping mode affects the way the winding current decays during the PWM off period.

There are four selectable decay modes:
Fast decay, Slow decay, Single-Mixed decay and Dual-Mixed decay.

In Fast decay mode the diagonal high-side and low-side transistors of the H-bridge are both switched off during the PWM off period causing the inductive current to be dissipated through the bypass diodes. The current decays in a direction opposing the motor supply voltage, resulting in fast decay.

In the Slow decay mode, the low side transistor of the H-bridge is switched off keeping the high side transistor on during the PWM off period. This causes the inductive current to recirculate through the high side transistor and diode loop. The current decays slowly because of the low loop voltage. The slow decay can be useful for motors that do not store enough energy in the windings leading to an average current too low for any useful torque.

In the Single-Mixed decay mode fast and slow decays are combined in the following way:

- When the motor is stationary, slow decay mode is applied to guarantee lowest current ripple in the holding state.

- When the motor is stepping, If the step requires the current in a winding to increase, slow decay is applied to the winding; if the step requires the current in a winding to decrease, fast-decay is applied followed by slow-decay after a programmable delay. Using fast-decay for transitioning to lower current level improves high speed response.

- In the Dual-Mixed decay mode, mixed decay will simultaneously be applied to both windings at all times.

One of six stepping modes can be selected by two input pins: Full, 1/2, 1/4, 1/8, 1/16 or 1/32. An internal oscillator generates the system clock and sets the PWM period. The oscillator pin can also be driven by an external clock. Other available inputs are for step command, stepping direction control, resetting to home, disabling H-bridge drives, sense input blanking delay control and fast-to-slow-decay delay control in the mixed-decay mode.

INPUT/OUTPUT DESCRIPTION

Rx, CLK, Cx

These three pins can be configured in one of three ways to obtain the system clock. A crystal connected between Rx and CLK pins or a resistor-capacitor pair connected among all three pins (see Fig 4) set the internal oscillator frequency. Alternatively, the CLK pin can be driven by an external clock. When configured as an RC oscillator, the frequency is given by: fosc = 1/(2RC). The system clock determines the maximum PWM pulse-width and is given by:
Tpwm = Tosc x 256, where Tosc is the oscillator period.

M0, M1
M0 is a 3-state input and M1 is a 2-state input, together they select the stepping mode as follows:

M1	M0	Stepping Mode
0	0	Full Step
1	0	1/2 Step
0	float	1/4 Step
1	float	1/8 Step
0	1	1/16 Step
1	1	1/32 Step

$\overline{\text{RESET}}$
When low the $\overline{\text{RESET}}$ input resets the PWM table pointer to HOME position per Table 2. This input has an internal pull-up resistor.

$\overline{\text{STEP}}$
A low pulse at the $\overline{\text{STEP}}$ input causes the motor to advance one step.

FRD/$\overline{\text{REV}}$
When high, this input causes the motor to step in the forward direction per incremental step sequences of table 2; when low it causes the motor to step in the reverse direction.

$\overline{\text{ENABLE}}$
When high, this input causes all motor drive outputs to be disabled by bringing $\overline{\text{INH1}}$, $\overline{\text{INH2}}$, PHA, PHB, PHC and PHD low; when low, it causes all motor drive outputs to be enabled.

HOME
Output to indicate Step0 position per table 2 with an active low.

VREF
Input for the chopper circuit DAC reference voltage which determines the peak motor winding current by regulating the PWM duty cycle. The DAC modifies the VREF input for the current sensing comparators at every step per table 2 and can be estimated as follows:

Vsens1 = | (VREF/7) x cos((90/32) x n)° |
and Vsens2 = | (VREF/ 7) x sin((90/32) x n)° |
where, n is the 1/32 step number per table 2.

The sense resistors should satisfy the relation:

Rs1 = Rs2 = VREF/(7 x Imax)
where Imax is the maximum motor winding current.

VREFH
Input for the reference voltage for controlling the holding torque when the holding-torque mode is enabled. The holding reference voltage should satisfy the relation:

VREFH = 7 x Rs1 x Imaxh = 7 x Rs2 x Imaxh
where, Imaxh is the maximum winding current intended in the holding state.

SENSE1, SENSE2
Inputs for motor winding current sense. A fractional-Ohm resistor connected in series with each of the H-bridge drivers produce SENSE1 and SENSE2 voltages. These voltages are compared with DAC modulated VREF voltages for generating the PWM phase or inhibit outputs.

PHA, PHB, PHC, PHD
Phase drive outputs for power stages. In a Bipolar motor PHA and PHB are used for one H-bridge while PHC and PHD are used for the other. In the Slow Decay Mode, the phase outputs are chopped with the current sense comparators.

$\overline{\text{INH1}}$, $\overline{\text{INH2}}$
These outputs are active low inhibit controls for motor drive outputs. $\overline{\text{INH1}}$ controls driver stage using PHA and PHB signals while $\overline{\text{INH2}}$ controls driver stage using PHC and PHD signals. In Fast Decay mode, inhibit outputs are chopped with the current sense comparators. In the Slow Decay mode, the inhibit outputs are driven high allowing for phase chopping.

$\overline{\text{SYNC}}$ Output
This open drain output produces a negative-going pulse occurring at the beginning of every PWM cycle which can be used to drive an external slope compensation scheme. Pulse width equals 3.2us at F_C = 5MHz.

Slope compensation is generally only needed at PWM levels exceeding 50%, particularly when fast decay is selected (DCYM = 1, TDCY1 = 0)

TBLNK
A resistor-capacitor pair connected to the TBLNK input controls the delay for which the sense comparator sampling is inhibited following the start of a PWM cycle.
The delay is given by:
TbInk = 1.2RbCb, where Rb and Cb are the resistor and the capacitor connected to the TBLNK pin.

THLD
A resistor-capacitor pair connected to this pin starts a timeout delay at every step command. At the start of the delay, the reference voltage at the VREF pin is switched in for the SENSE comparators to produce higher stepping torque. At the end of the timeout, the reference voltage at the VREFH pin is switched in for the SENSE comparators to produce the lower holding torque, reducing the power dissipation while the motor is stationary.
The delay is given by:
THLD = $1.4R_HC_H$, where R_H and C_H are the resistor and capacitor connected to the THLD pin.

If the pin is tied low, holding torque mode is disabled and the stepping torque is produced in both dynamic and static conditions by using the VREF input for the reference voltage.

V_{SS}
Supply negative terminal.

V_{DD}
Supply positive terminal.

DCYM, TDCY1, TDCY2
For the **LS8290**, DCYM and TDCY1 pins are used to control the PWM decay modes. One of three decay modes can be selected as follows:

DCYM	TDCY1	Decay Mode
1	0	Fast decay
1	1	Slow decay
0	R_1C_1	Single-Mixed decay

For the LS8291, DCYM, TDCY1 and TDCY2 pins are used to select one of four decay modes as follows:

DCYM	TDCY1	TDCY2	Decay Mode
1	0	x	Fast decay
1	1	x	Slow decay
0	R_1C_1	0	Single-Mixed decay
0	R_1C_1	R_2C_2	Dual-Mixed decay

In the Fast decay mode $\overline{\text{INH1}}$ and $\overline{\text{INH2}}$ outputs are chopped.
In the Slow decay mode PHA, PHB, PHC and PHD outputs are chopped.

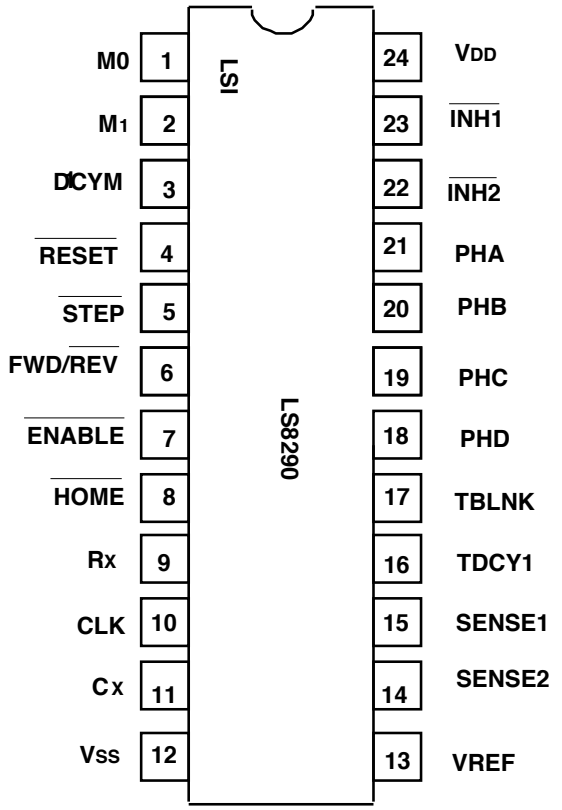
(continued on next page)

In the Single-Mixed decay mode with a resistor-capacitor pair connected to the TDCY1 pin controls the duration of fast decay before switching to slow decay for the winding requiring a transition to a lower current following a micro-step. The delay is given by $Tdcy1 = 1.2R_1C_1$, where R_1 and C_1 are the resistor and capacitor connected to the TDCY1 pin. Slow decay is applied to the winding requiring a transition to a higher current. At standstill, slow decay is applied to both windings. In the Dual-Mixed decay mode both windings undergo mixed-decay every PWM cycle in which fast-decay is followed by slow-decay after the programmed delay.

The delays for the two windings are:

$Tdcy1 = 1.2R_1C_1$, $Tdcy2 = 1.2R_2C_2$, where R_1C_1 and R_2C_2 are resistors and capacitors connected to TDCY1 and TDCY2, respectively.

PIN ASSIGNMENT
TOP VIEW



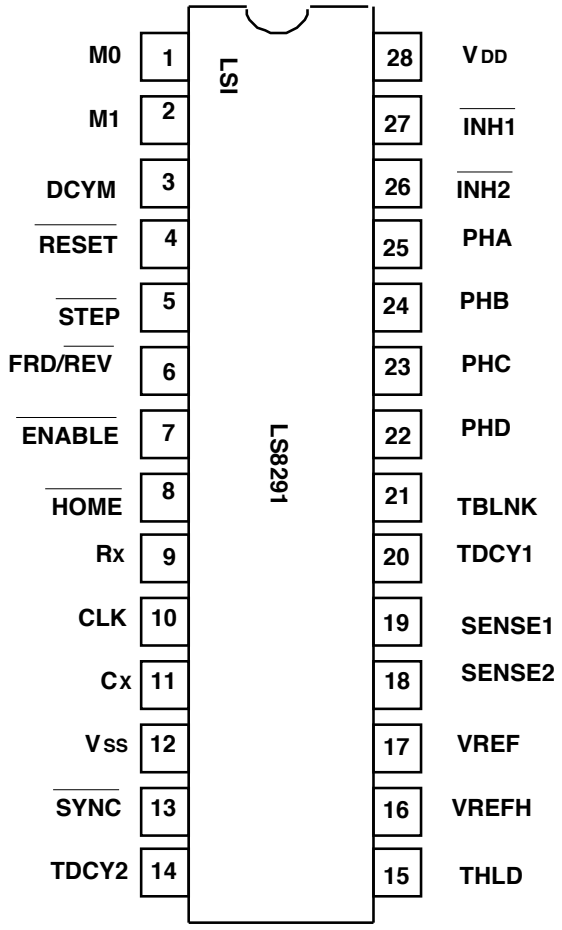


FIGURE 1

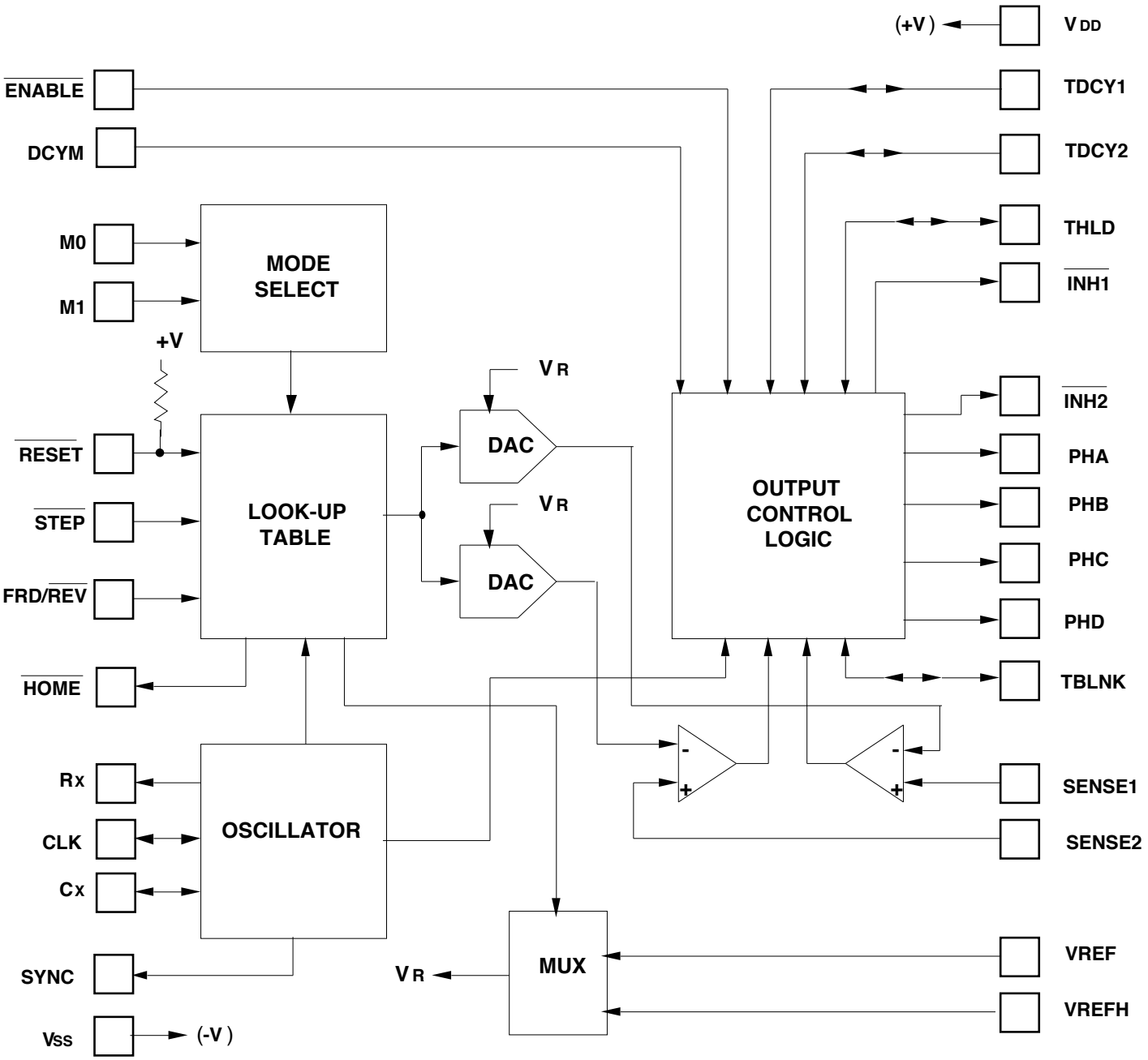


FIGURE 2. LS8290 / LS8291 BLOCK DIAGRAM

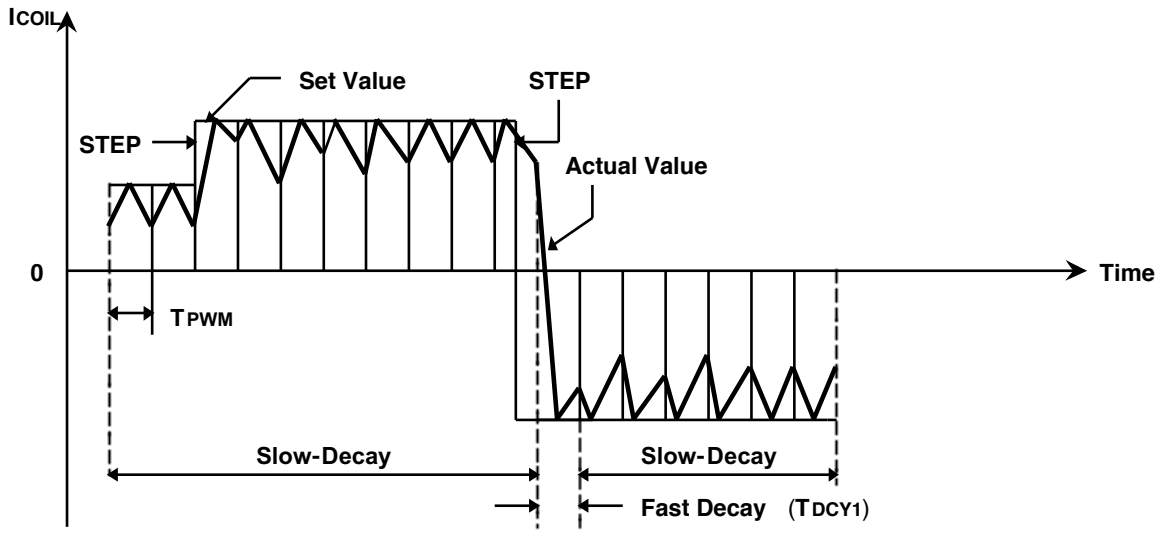


FIGURE 3. Mixed-Decay PWM

NOTE: Mixed decay is applied to a winding transitioning to a lower current and slow decay is applied to a winding transitioning to a higher current.

ABSOLUTE MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage	V_{DD} - V_{SS}	+7	V
Any Input Voltage	V_{IN}	V_{SS} - 0.3 to V_{DD} + 0.3	V
Operating Temperature	T_A	-20 to +85	^oC
Storage Temperature	T_{STG}	-65 to +125	^oC

ELECTRICAL SPECIFICATIONS (-25^{o}C < T_A < +85^{o}C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Supply Voltage	V_{DD}	4.5	-	5.5	V	-
Suppy Current	I_{DD}	-	-	500	uA	Outputs floating, Inputs high
CLK frequency	f_C	-	5.00	8.00	MHz	-
ENABLE Propagation Delay	t_{epd}	100	-	-	ns	-
FRD/RVRS Setup Time (before step pulse)	tds	0	-	-	us	-
Step Pulse Width	SPW	1.6	-	-	us	at f_C = 5MHz
PWM Period	T_{PWM}	-	256/f_C	-	us	-
Reset Pulse Width	R_{PW}	1.6	-	-	us	at f_C = 5MHz
Reset to Step Pulse Delay	t_{rs}	0	-	-	us	-
Hi-Level Input Voltage	V_{IH}	2	-	-	V	V_{DD} = 5V ± 0.25V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V	V_{DD} = 5V ± 0.25V
All Other Inputs:						
Hi-Level Input Current	I_H	-	-	50	nA	Leakage Current
Low-Level Input Current	I_L	-	-	50	nA	Leakage Current
Reset input current:						
High	I_{RH}	-	-	30	uA	VR = 2V
Low	I_{RL}	-	-	40	uA	VR = 0.8V
All Outputs:						
Output Sink Current	I_O	-10	-	-	mA	V_O = 0.4V, V_{DD} = 5V
Output Source Current	I_O	5	-	-	mA	V_O = 4.0V, V_{DD} = 5V
Comparator Offset Volt.	V_{OS}	-	50	200	uV	V_{REF} = 2V
Input Reference Volt.	V_{REF}, V_{REFH}	2.5	-	4.5	V	V_{DD} = 5V

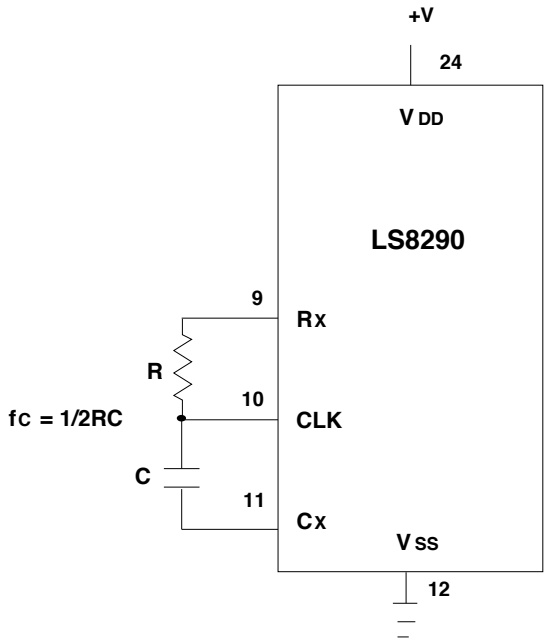
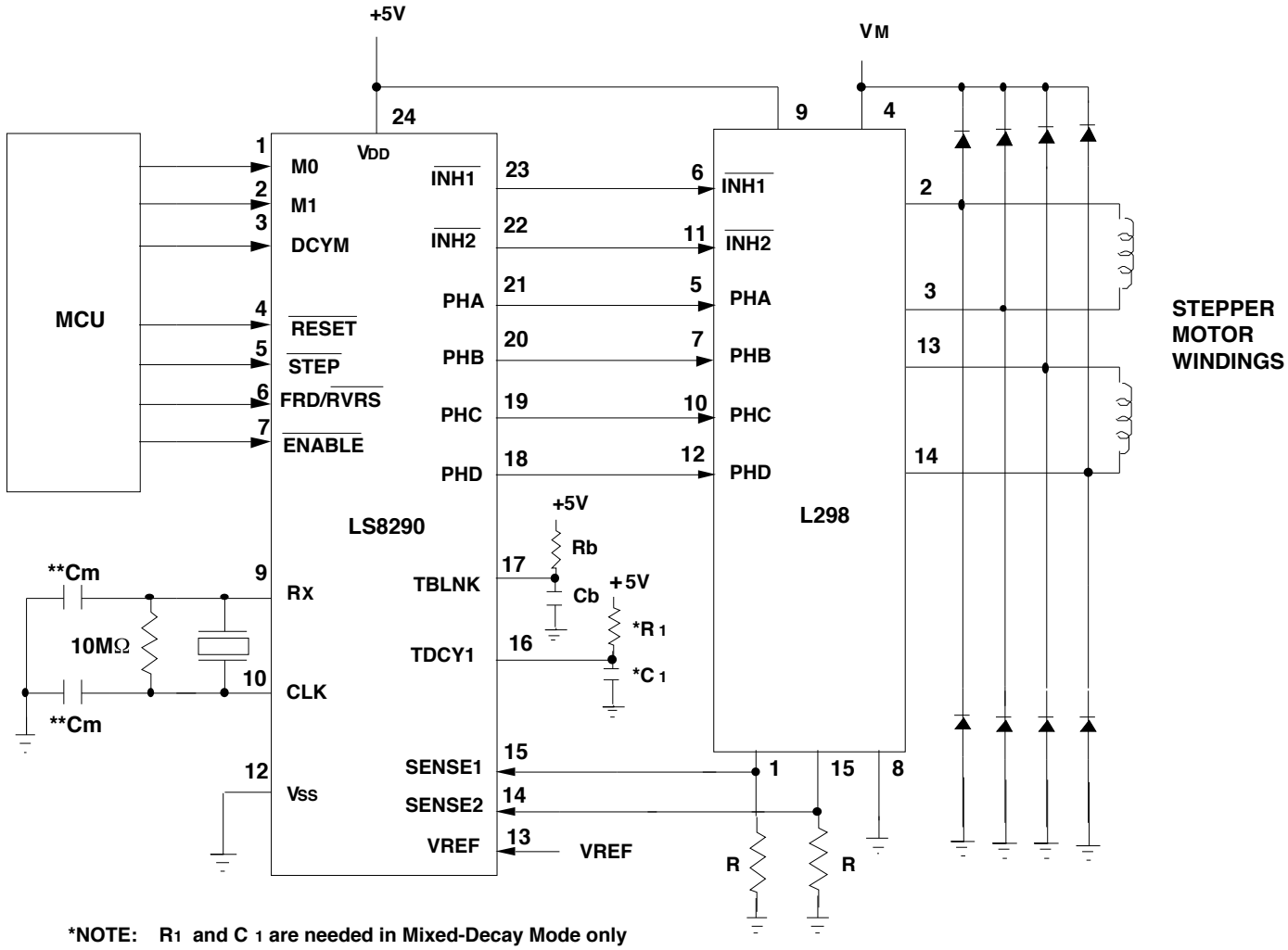


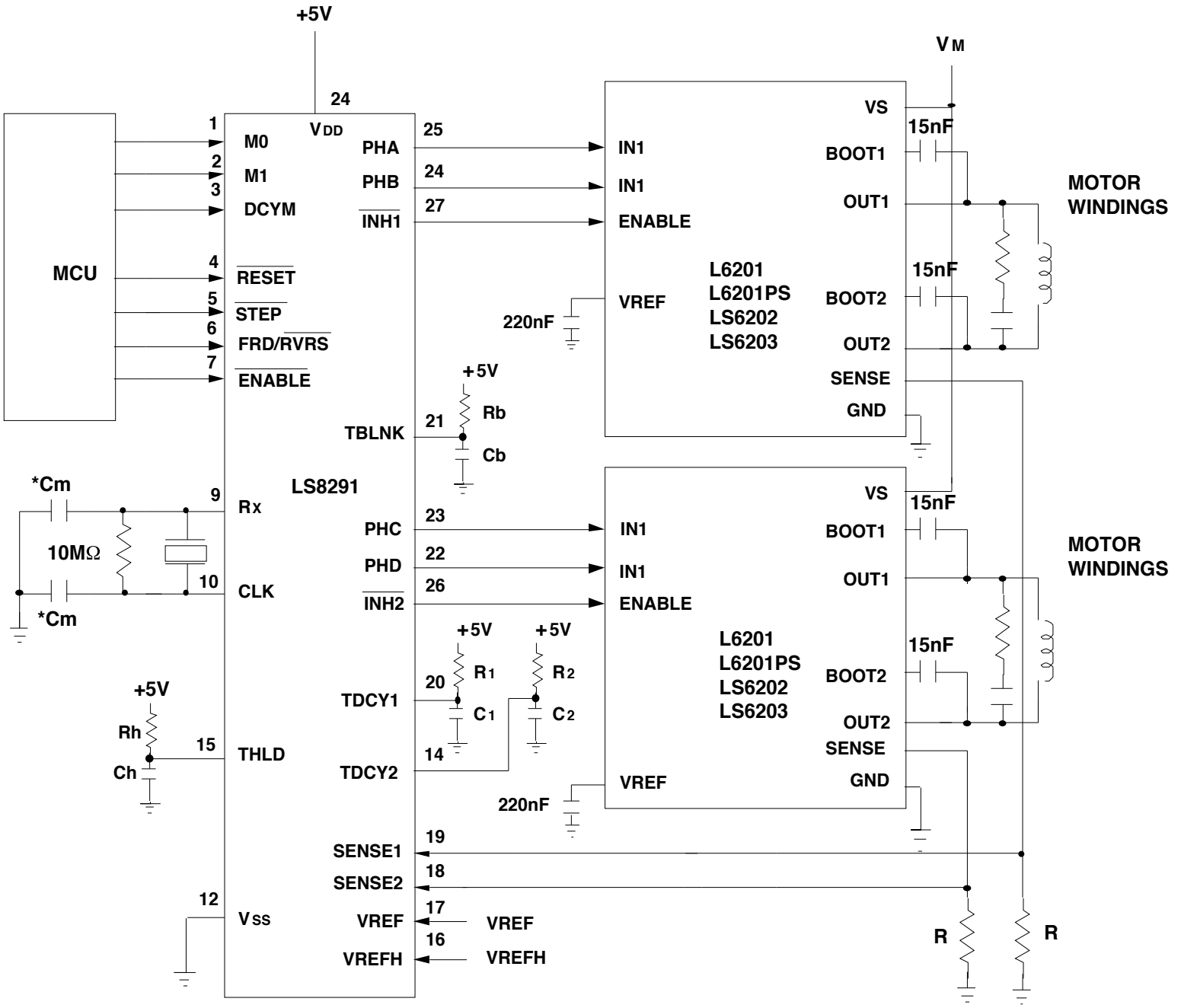
FIGURE 4. LS8290 RC OSCILLATOR FOR CLOCK GENERATOR



*NOTE: R_1 and C_1 are needed in Mixed-Decay Mode only

**NOTE: Cm is chosen according to the following relation:
$Cm = 2(C_L - C_P) - 10pF$, where
C_L = crystal load capacitance
C_P = parasitic capacitance

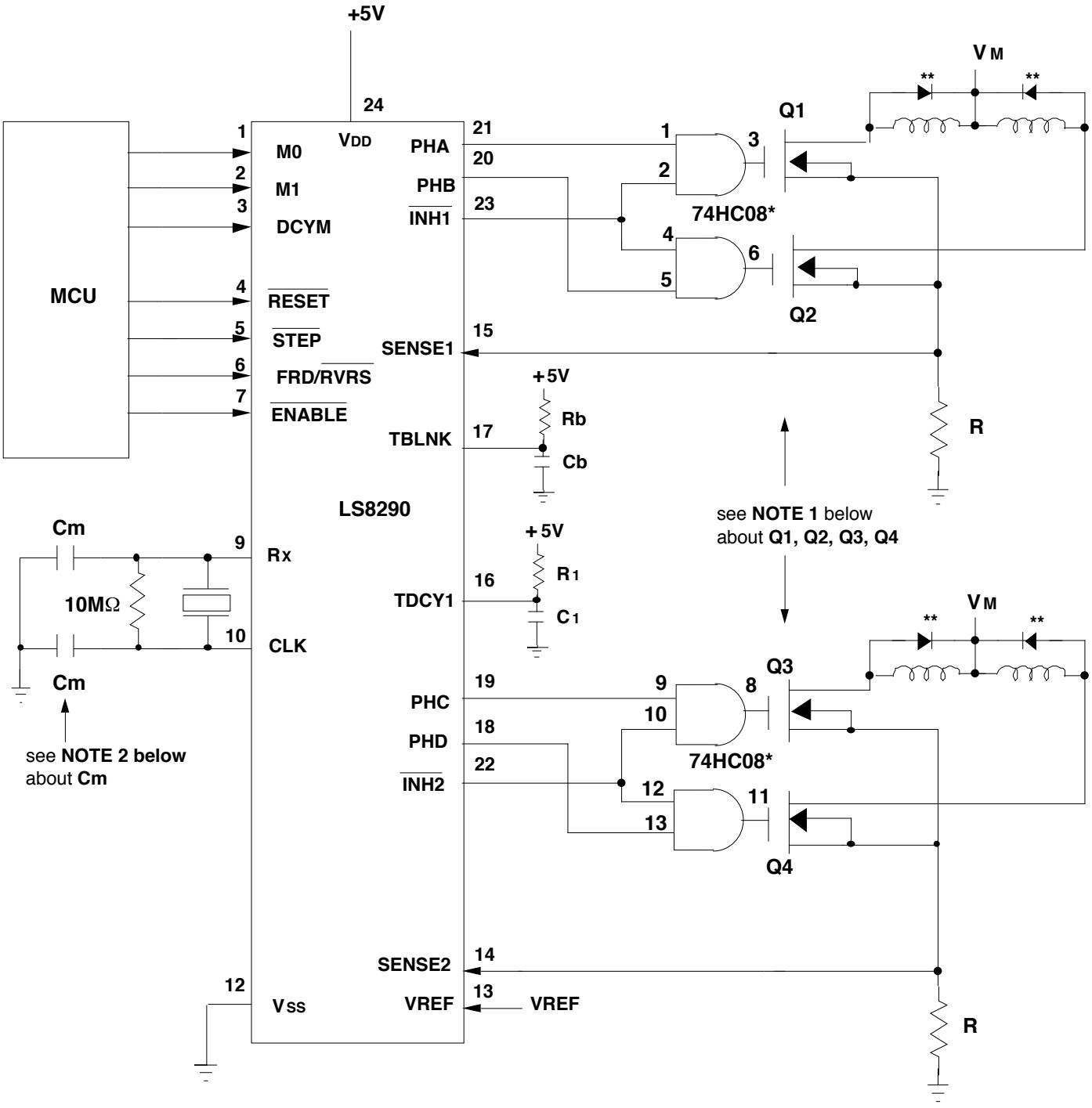
FIGURE 5. LS8290 APPLICATION SCHEMATIC FOR A TWO-PHASE BIPOLAR MOTOR USING A SINGLE MOTOR DRIVER IC



NOTE: All functional options have been implemented in this application example.
The following components may be eliminated if all options are not used:
- R_1, R_2 and C_1, C_2 if Mixed-Decay mode is not used.
TDCY1 pin must be tied to +V or ground and DCYM is tied to +V if Mixed-Decay is disabled.
- Rh and Ch and the reference VREFH if holding-torque mode is not used.
To disable holding torque, the THLD pin must be tied to ground.

***NOTE: Cm is chosen according to the following relation:**
$Cm = 2(C_L - C_P) - 10pF$, where
C_L = crystal load capacitance
C_P = parasitic capacitance

FIGURE 6. LS8291 APPLICATION SCHEMATIC FOR A TWO-PHASE BIPOLAR MOTOR USING TWO SEPARATE MOTOR DRIVER ICs



NOTE 1: Q1, Q2, Q3, Q4 are MOSFET Power Transistors suitable for 5V GATE DRIVE
Typical P/Ns = IRLZ44N and IRF3708

NOTE 2: Cm is chosen according to the following relation:
$C_m = 2(C_L - C_P) - 10pF$, where
C_L = crystal load capacitance
C_P = parasitic capacitance

***NOTE: For higher pre-drive capability, the 74CH08 can be replaced by the MIC4468**

****NOTE: Depending on the motor selected, the diodes across the motor windings may be eliminated to enable Fast decay. With the diodes present, Slow decay occurs.**

FIGURE 7. TYPICAL APPLICATION SCHEMATIC FOR A FOUR-PHASE UNIPOLAR MOTOR USING DISCRETE MOSFET TRANSISTORS

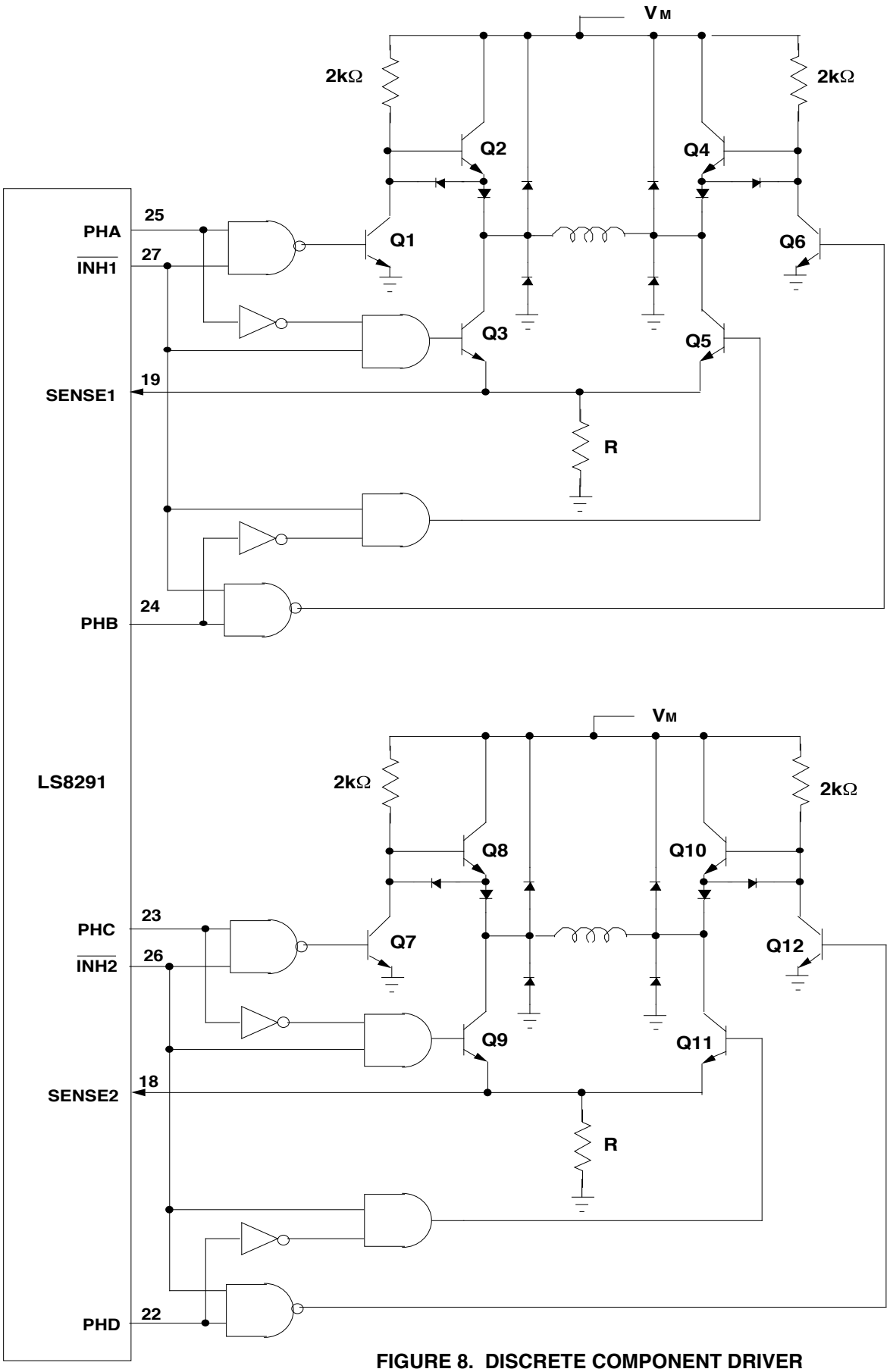


FIGURE 8. DISCRETE COMPONENT DRIVER

(Supports up to 4A/Winding, 80V Motors)

NOTE: All Inverters = 74HC04
All Inverting Gates = 74HC00
All Non-Inverting Gates = 74HC08

Diodes across Base-to-Emitter junctions of Q2, Q4, Q8 and Q10 = 1N4148
All other Diodes = 6A10
Q1 = Q6 = Q7 = Q12 = 2N5551
Q2 = Q3 = Q4 = Q5 = Q8 = Q9 = Q10 = Q11 = BD679

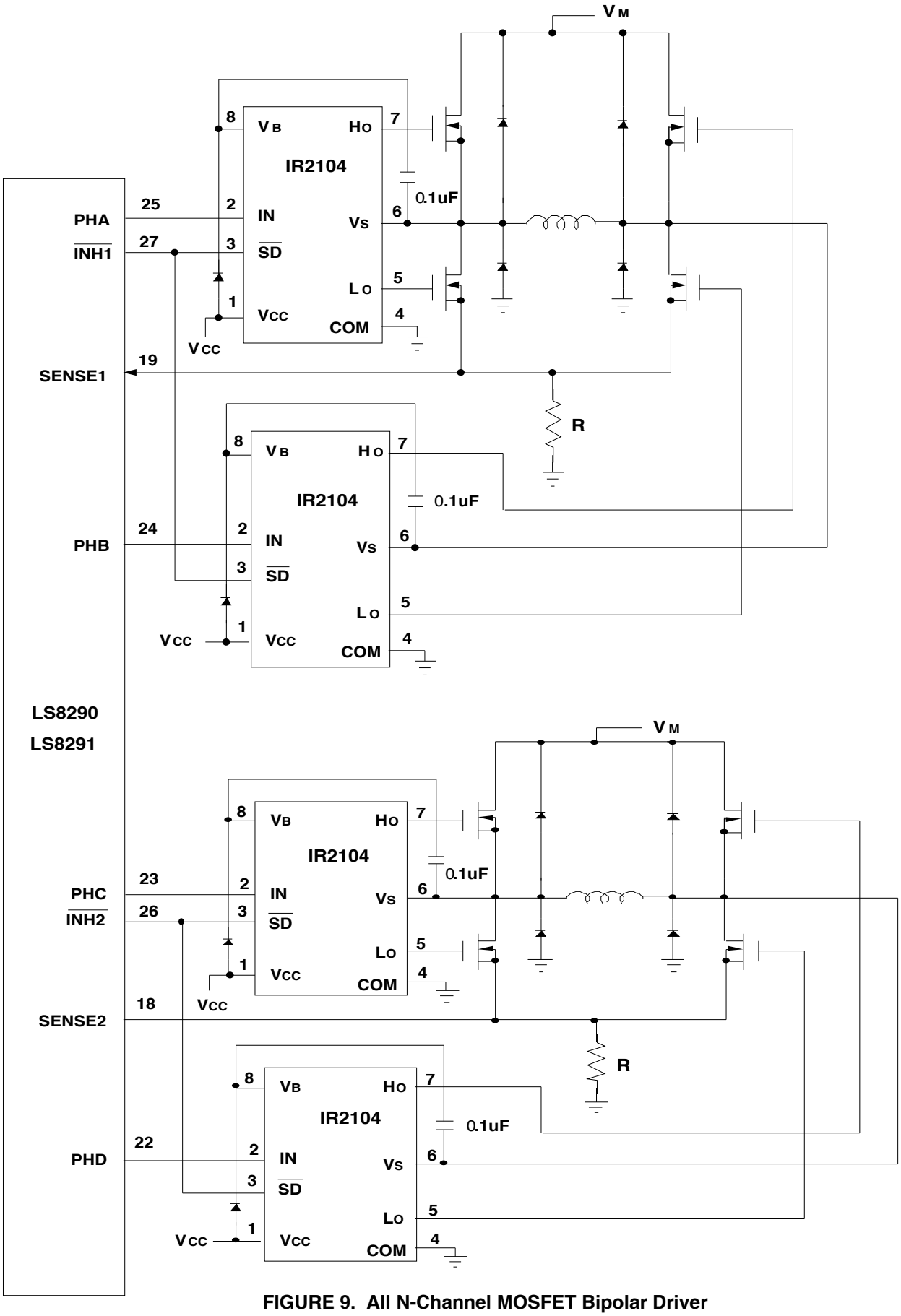


FIGURE 9. All N-Channel MOSFET Bipolar Driver

NOTE: Using the IR2104 Half-Bridge Driver for interfacing the LS8290 / LS8291 with an all N-Channel MOSFET Bipolar Motor Driver for motors up to 600V. With V_{CC} set to 20V and $V_M \leq$ 100V, suggested NMOS FETs are IRF540N and suggested Diodes are 1N4002.

TABLE 2

Step Number						% Duty Cycle (PWM)		Phases				
Full	1/2	1/4	1/8	1/16	1/32	$\overline{INH1}$	$\overline{INH2}$	PHA	PHB	PHC	PHD	Step Angle
0	0	0	0	0	0	100.0	0.0	1	0	1	0	HOME
					1	99.9	4.9	1	0	1	0	2.81
				1	2	99.5	9.8	1	0	1	0	5.63
					3	98.9	14.7	1	0	1	0	8.44
			1	2	4	98.1	19.5	1	0	1	0	11.25
					5	97.0	24.3	1	0	1	0	14.06
				3	6	95.7	29.0	1	0	1	0	16.88
					7	94.2	33.7	1	0	1	0	19.69
		1	2	4	8	92.4	38.3	1	0	1	0	22.50
					9	90.4	42.8	1	0	1	0	25.31
				5	10	88.2	47.1	1	0	1	0	28.13
					11	85.8	51.4	1	0	1	0	30.94
			3	6	12	83.1	55.6	1	0	1	0	33.75
					13	80.3	59.6	1	0	1	0	36.56
				7	14	77.3	63.4	1	0	1	0	39.38
					15	74.1	67.2	1	0	1	0	42.19
	1	2	4	8	16	70.7	70.7	1	0	1	0	45.00
					17	67.2	74.1	1	0	1	0	47.81
				9	18	63.4	77.3	1	0	1	0	50.63
					19	59.6	80.3	1	0	1	0	53.44
			5	10	20	55.6	83.1	1	0	1	0	56.25
					21	51.4	85.8	1	0	1	0	59.06
				11	22	47.1	88.2	1	0	1	0	61.88
					23	42.8	90.4	1	0	1	0	64.69
		3	6	12	24	38.3	92.4	1	0	1	0	67.50
					25	33.7	94.2	1	0	1	0	70.31
				13	26	29.0	95.7	1	0	1	0	73.13
					27	24.3	97.0	1	0	1	0	75.94
			7	14	28	19.5	98.1	1	0	1	0	78.75
					29	14.7	98.9	1	0	1	0	81.56
				15	30	9.8	99.5	1	0	1	0	84.38
					31	4.9	99.9	1	0	1	0	87.19
1	2	4	8	16	32	0.0	100.0	0	1	1	0	90.00
					33	4.9	99.9	0	1	1	0	92.81
				17	34	9.8	99.5	0	1	1	0	95.63
					35	14.7	98.9	0	1	1	0	98.44
			9	18	36	19.5	98.1	0	1	1	0	101.25
					37	24.3	97.0	0	1	1	0	104.06
				19	38	29.0	95.7	0	1	1	0	106.88

NOTE: In Table 2, the PWM duty cycles are indicated for the Fast Decay mode where the $\overline{INH1}$ and $\overline{INH2}$ outputs are chopped. In the Slow Decay mode, these two outputs remain high while the Phase outputs are chopped.

TABLE 2 (continued)

Step Number						% Duty Cycle (PWM)		Phases				
Full	1/2	1/4	1/8	1/16	1/32	$\overline{INH1}$	$\overline{INH2}$	PHA	PHB	PHC	PHD	Step Angle
					39	33.7	94.2	0	1	1	0	109.69
		5	10	20	40	38.3	92.4	0	1	1	0	112.50
					41	42.8	90.4	0	1	1	0	115.31
				21	42	47.1	88.2	0	1	1	0	118.13
					43	51.4	85.8	0	1	1	0	120.94
			11	22	44	55.6	83.1	0	1	1	0	123.75
					45	59.6	80.3	0	1	1	0	126.56
				23	46	63.4	77.3	0	1	1	0	129.38
					47	67.2	74.1	0	1	1	0	132.19
	3	6	12	24	48	70.7	70.7	0	1	1	0	135.00
					49	74.1	67.2	0	1	1	0	137.81
				25	50	77.3	63.4	0	1	1	0	140.63
					51	80.3	59.6	0	1	1	0	143.44
			13	26	52	83.1	55.6	0	1	1	0	146.25
					53	85.8	51.4	0	1	1	0	149.06
				27	54	88.2	47.1	0	1	1	0	151.88
					55	90.4	42.8	0	1	1	0	154.69
		7	14	28	56	92.4	38.3	0	1	1	0	157.50
					57	94.2	33.7	0	1	1	0	160.31
				29	58	95.7	29.0	0	1	1	0	163.13
					59	97.0	24.3	0	1	1	0	165.94
			15	30	60	98.1	19.5	0	1	1	0	168.75
					61	98.9	14.7	0	1	1	0	171.56
				31	62	99.5	9.8	0	1	1	0	174.38
					63	99.9	4.9	0	1	1	0	177.19
2	4	8	16	32	64	100.0	0.0	0	1	0	1	180.00
					65	99.9	4.9	0	1	0	1	182.81
				33	66	99.5	9.8	0	1	0	1	185.63
					67	98.9	14.7	0	1	0	1	188.44
			17	34	68	98.1	19.5	0	1	0	1	191.25
					69	97.0	24.3	0	1	0	1	194.06
				35	70	95.7	29.0	0	1	0	1	196.88
					71	94.2	33.7	0	1	0	1	199.69
		9	18	36	72	92.4	38.3	0	1	0	1	202.50
					73	90.4	42.8	0	1	0	1	205.31
				37	74	88.2	47.1	0	1	0	1	208.13
					75	85.8	51.4	0	1	0	1	210.94
			19	38	76	83.1	55.6	0	1	0	1	213.75
					77	80.3	59.6	0	1	0	1	216.56
				39	78	77.3	63.4	0	1	0	1	219.38
					79	74.1	67.2	0	1	0	1	222.19
	5	10	20	40	80	70.7	70.7	0	1	0	1	225.00
					81	67.2	74.1	0	1	0	1	227.81
				41	82	63.4	77.3	0	1	0	1	230.63
					83	59.6	80.3	0	1	0	1	233.44

TABLE 2 (continued)

Step Number						% Duty Cycle (PWM)		Phases				
Full	1/2	1/4	1/8	1/16	1/32	$\overline{INH1}$	$\overline{INH2}$	PHA	PHB	PHC	PHD	Step Angle
			21	42	84	55.6	83.1	0	1	0	1	236.25
					85	51.4	85.8	0	1	0	1	239.06
				43	86	47.1	88.2	0	1	0	1	241.88
					87	42.8	90.4	0	1	0	1	244.69
		11	22	44	88	38.3	92.4	0	1	0	1	247.50
					89	33.7	94.2	0	1	0	1	250.31
				45	90	29.0	95.7	0	1	0	1	253.13
					91	24.3	97.0	0	1	0	1	255.94
			23	46	92	19.5	98.1	0	1	0	1	258.75
					93	14.7	98.9	0	1	0	1	261.56
				47	94	9.8	99.5	0	1	0	1	264.38
					95	4.9	99.9	0	1	0	1	267.19
3	6	12	24	48	96	0.0	100	1	0	0	1	270.00
					97	4.9	99.9	1	0	0	1	272.81
				49	98	9.8	99.5	1	0	0	1	275.63
					99	14.7	98.9	1	0	0	1	278.44
			25	50	100	19.5	98.1	1	0	0	1	281.25
					101	24.3	97.0	1	0	0	1	284.06
				51	102	29.0	95.7	1	0	0	1	286.88
					103	33.7	94.2	1	0	0	1	289.69
		13	26	52	104	38.3	92.4	1	0	0	1	292.50
					105	42.8	90.4	1	0	0	1	295.31
				53	106	47.1	88.2	1	0	0	1	298.13
					107	51.4	85.8	1	0	0	1	300.94
			27	54	108	55.6	83.1	1	0	0	1	303.75
					109	59.6	80.3	1	0	0	1	306.56
				55	110	63.4	77.3	1	0	0	1	309.38
					111	67.2	74.1	1	0	0	1	312.19
	7	14	28	56	112	70.7	70.7	1	0	0	1	315.00
					113	74.1	67.2	1	0	0	1	317.81
				57	114	77.3	63.4	1	0	0	1	320.63
					115	80.3	59.6	1	0	0	1	323.44
			29	58	116	83.1	55.6	1	0	0	1	326.25
					117	85.8	51.4	1	0	0	1	329.06
				59	118	88.2	47.1	1	0	0	1	331.88
					119	90.4	42.8	1	0	0	1	334.69
		15	30	60	120	92.4	38.3	1	0	0	1	337.50
					121	94.2	33.7	1	0	0	1	340.31
				61	122	95.7	29.0	1	0	0	1	343.13
					123	97.0	24.3	1	0	0	1	345.95
			31	62	124	98.1	19.5	1	0	0	1	348.75
					125	98.9	14.7	1	0	0	1	351.56
				63	126	99.5	9.8	1	0	0	1	354.38
					127	99.9	4.9	1	0	0	1	357.19
0	0	0	0	0	0	100.0	0.0	1	0	1	0	HOME