

TYPEC/PD2.0/PD3.0 Physical Layer IC for USB TYPEC input Interfaces

1. Features

- Support TYPEC/PD2.0/PD3.0 UFP mode for USB TYPEC input port
 - > Auto-detect USB connection condition
- Integrate USB Power Delivery (PD2.0/PD3.0)
 protocol
 - Integrate hardware bi-phase Mark Coding (BMC) over CC
 - Integrate physical layer
 - Hardware CRC protect data integrity
 - Integrate PD2.0/PD3.0 protocol UFP engine
 - Support hardreset
- Integrate USB TYPEC protocol
- Power management
 - VBUSG control the power rail by the external NMOS, depending on CC negotiation state
 - IP2721: SEL configure the maximum PD request voltage as 20V, 15V or 5V
 - IP2721_MAX12: SEL configure the maximum PD request voltage as 12V, 9V or 5V
- Support VBUS soft start

4. Typical Application Schematic

- Working voltage: 3V~25V
- Package: TSSOP16

2. Description

IP2721 is a USB TYPEC/PC2.0/PD3.0 physical layer protocol IC for USB TYPEC input port, support auto-detect USB port connection through CC1 and CC2. Integrate hardware PD protocol, analyze PD protocol to get source capabilities and request appropriate voltage accordingly.

3. Typical Applications

• USB TYPEC input port for Power Banka, cell phone, wireless charging dock, VR box and UAV etc.





5. PIN Description



TSSOP16

Pin No.	Pin Name		Description				
1	VBUSG	Connect to the gate of external NMOS, in control of the power rail.					
2	VIN		Power input pin, apply 1uF capacitor to GND, connect to the Drain of the external NMOS.				
3,4	NC	Keep floating					
5	GND	Ground					
6,7,8	TST1/TST2/TST2	Reserved PIN	Reserved PIN, keep floating				
9,10	NC	Keep floating					
	SEL		IP2721	IP2721_MAX12			
11		High:	20V	12V			
11	SEL	Floating:	15V	9V			
		GND:	5V	5V			
12	CC2	Connect to Co	C2 of USB Typ	e-C port			
13	CC1	Connect to CC1 of USB Type-C port					
14,15	NC	Keep floating					
16	VBUS	Connect to th	e source of e	xternal NMOS			



6. IP Series Products List

USB Charging Port Control IC

						Stand	ards su	upported				Pack	age
IC Part No.	Cha nnel	BC1.2 & APPLE	QC3.0 & QC2.0	FCP	SCP	AFC	SFCP	MTK PE+ 2.0&1.1	ТуреС	NTC	PD2.0/ PD3.0/PPS	Package	Compati bility
IP2110	1	٧	-	-	-	-	-	-	-	-	-	SOT23-5	
IP2111 IP2111A	1	٧	-	-	-	-	-	-	-	-		SOT23-6	
IP2112 IP2112A	2	v	-	-	-	-	-	-	-	- (SOT23-6	
IP2161	1	٧	٧	٧	-	٧	٧	-	-	-		SOT23-6	
IP2163	1	٧	٧	٧	-	٧	٧	v	-	v	-	SOP8	PIN2 PIN
IP2183	1	٧	٧	٧	v	٧	٧	V	-		-	SOP8	II
IP2701	1	٧	٧	٧	-	٧	٧		v	-	-	SOP8	
IP2703	1	٧	٧	٧	-	٧	۷	V	٧	٧	-	DFN10	
IP2705	1	٧	٧	٧	-	V	V	V	v	٧	-	DFN12	
IP2707	2	٧	٧	٧	-	V	~	V	v	٧	-	QFN16	
IP2712	1	٧	٧	٧	٧	1	-	1.1	v	-	v	TSSOP20L	
IP2716	1	٧	٧	٧	۷	V	-	1.1	٧	-	v	QFN32	
IP2723	1	٧	٧	٧	٧	~	٧	v	٧	-	v	TSSOP16	
IP2721	1	-	C	-			-	-	-	-	√ SINK	TSSOP16	

7. Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
VIN input voltage range	VIN	-0.3 ~ 30	v
CC1,CC2 input voltage range	V _{CC1} ,V _{CC2}	-0.3 ~ 30	v
Other pins voltage range		-0.3 ~ 10	v
Junction temperature range	TJ	-40 ~ 150	Ĉ
Storage temperature	Tstg	-60 ~ 150	Ĉ
Lead temperature (Soldering, 10sec.)	Ts	260	C
Ambient temperature range	T _A	-40~120	Ĉ



Package thermal resistance	θ_{JA}	90	°C /w
Package thermal resistance	θις	39	°C/w
Human body model (HBM)	ESD	2	KV

*Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

*Voltages are referenced to GND unless otherwise noted.

8. Recommended Operating Conditions

Parameter	Symbol	Min.	Тур.	Max.	Unit
	eyee		.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		
Input voltage	VIN	3		25	V
Ambient temperature	T _A	-40		85	°C

*Devices' performance cannot be guaranteed when working beyond those Recommended Operating Conditions.

9. Electrical Characteristics

Unless otherwise specified, T A =25 $^\circ C$, 4.5V \leq VCC1 \leq 5.5V

Parameter	Symbol	Test Condition	Min.	Тур.	Max.	Unit
Input voltage	VIN	Supplied directly	3		25	V
Input UVLO threshold	UVLO	VIN Falling	2.5		2.9	V
Quiescent current	Ιq	CC floating	120		145	uA
	lų	CC connected	1		1.5	mA
Start time	Ts		20	37	50	us
VBUS soft start time	Τv		3.5		4.5	ms
SEL input high voltage threshold	V _{SELH}		2.5			V
SEL input low voltage threshold	V _{SELL}				0.3	V
SEL default output voltage	V _{SELO}		1.35	1.5	1.65	V
CC1/CC2 connection detection	V _{CC1_TH} /		0.25		2.04	V
threshold voltage	$V_{CC2_{TH}}$		0.25		2.04	v



10.Function Description

USB TYPEC/PD protocol

IP2721 is an integrated USB TYPEC PD protocol IC for USB input port, support USB TYPEC/PD2.0/PD3.0 protocol. USB TYPEC device plug-in and plug-out is auto-detected based on CC1/CC2 pins. IP2721 integrated PD protocol analyzer to get the voltage capabilities and request the matched voltage.

- Port mode: sink (device)
- Auto-detect USB TYPEC device plug-in and plug-out
- Integrate hardware bi-phase Mark Coding (BMC) over CC
- Integrate physical layer
- Integrate PD protocol state machine
- Support PD hardreset

SEL pin

SEL pin is used to configure the maximum voltage that IP2721 will request, when SEL is pulled to high voltage level V_{SELH} , the maximum request voltage is 20V; when SEL is floating, the maximum voltage that IP2721 request is 15V; when SEL pull down to GND, IP2721 only request 5V voltage.

If the maximum voltage SRC port supported is lower than IP2721 capable of, IP2721 will request the maximum voltage supported by the SRC port. If the maximum voltage SRC port supported is higher than IP2721 capable of , IP2721 will request its maximum voltage and supported by the SRC port as well. That is to say, IP2721 will request the maximum voltage supported by both IP2721 and SRC port.

The customized models of IP2721_MAX is configured switching the maximum request voltage among 12V, 9V and 5V by SEL. SEL pull 100kohm resistor to VIN is V_{SELH}. The switching of SEL voltage level is not supported after power up, it should be connected well before IP2721 power up.

SEL	IP2721 Voltage	IP2721_MAX12 Voltage
V _{SELH}	20V	12V
Floating	15V	9V
GND	5V	5V

Power path control

IP2721 support external NMOS for power path control, controlling the Gate of external NMOS by VBUSG pin. The NMOS will be turned on when CC connection is established, and turned off when CC disconnected.

*Power NMOS of Vds withstand voltage above 30V is recommended.



11.Package







WITH PLATING



SYMBOL	MI	ILLIMET	ER
STMBOL	MIN	NOM	MAX
Α		_	1.20
A1	0.05		0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0,49
b	0.20	_	0.29
b1	0.19	0.22	0.25
c	0.13		0.18
cl	0.12	0.13	0.14
D	4.86	4.96	5.06
Е	6.20	6.40	6.60
El	4.30	4.40	4.50
e	(0.65BSC	
L	0.45	0.60	0.75
L1	1	1.00BSC	
θ	0		8°



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