# CR6842

## Green-Power PWM Controller with Freq. Jittering



### Features

- Low Cost, Green-Power Burst-Mode PWM
- Very Low Start-up Current ( about 7.5μA)
- Low Operating Current ( about 3.0mA)
- Current Mode Operation
- Under Voltage Lockout (UVLO)
- VDD Over Voltage Protection(OVP)
- programmable over-temperature protection
- Internal Latch Circuit(OTP,OVP)
- Built-in soft start with 1ms
- Built-in Frequency jitter for better EMI Signature
- Soft Clamped gate output voltage 16.5V
- VDD over voltage protect 25.5V
- Cycle-by-cycle current limiting
- Sense Fault Protection
- Output SCP (Short circuit Protection)
- Built-in Synchronized Slope Compensation
- Leading-edge blanking on Sense input
- Programmable PWM Frequency
- High-Voltage CMOS Process with ESD
- DIP-8 & SOP-8 Pb-Free Package
- **Compatible with SG6842J&LD7552&OB2269**

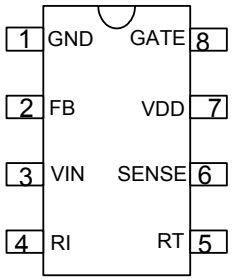
### Applications

- Power Adaptor
- Battery Charger Adapter
- Open Frame Switching Power Supply
- LCD Monitor

### General Description

The CR6842 is a low startup current , low cost, current mode PWM controller with Green-Power & burst-mode power-saving operation. The integrated functions such as the leading-edge blanking of the current sensing, internal slope compensation provide the users a high efficiency, low external component counts, and low cost solution for AC/DC power applications. The special Green-Power function provides off-time modulation to linearly decrease the switching frequency under light-load conditions. And under zero-load conditions, the power supply enters burst-mode to further reduce power consumption by shutting off PWM output. When the output of power supply is short or over loaded, the FB voltage will increase ,and if the FB voltage is higher than 5.2V for longer than 56msec the PWM output will be turned off. A external NTC resistor connected from pin RT to ground can be applied to over-temperature protection. Pulse by pulse current limit ensures a constant output current even under short circuit. PWM output will be disabled as long as VDD exceeds a threshold. When internal latch circuit is used to latch-off the controller, the latch will be reset when the power supply VDD is disabled.

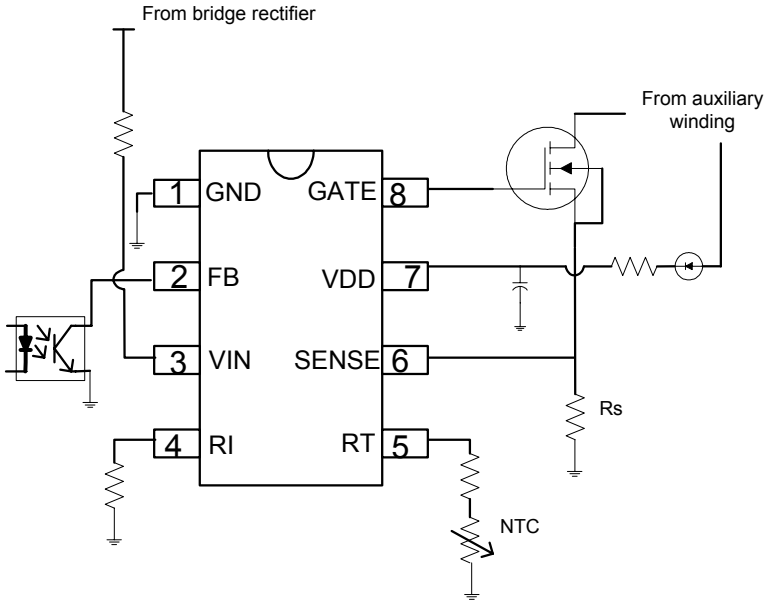
## Pin Assignment & Description



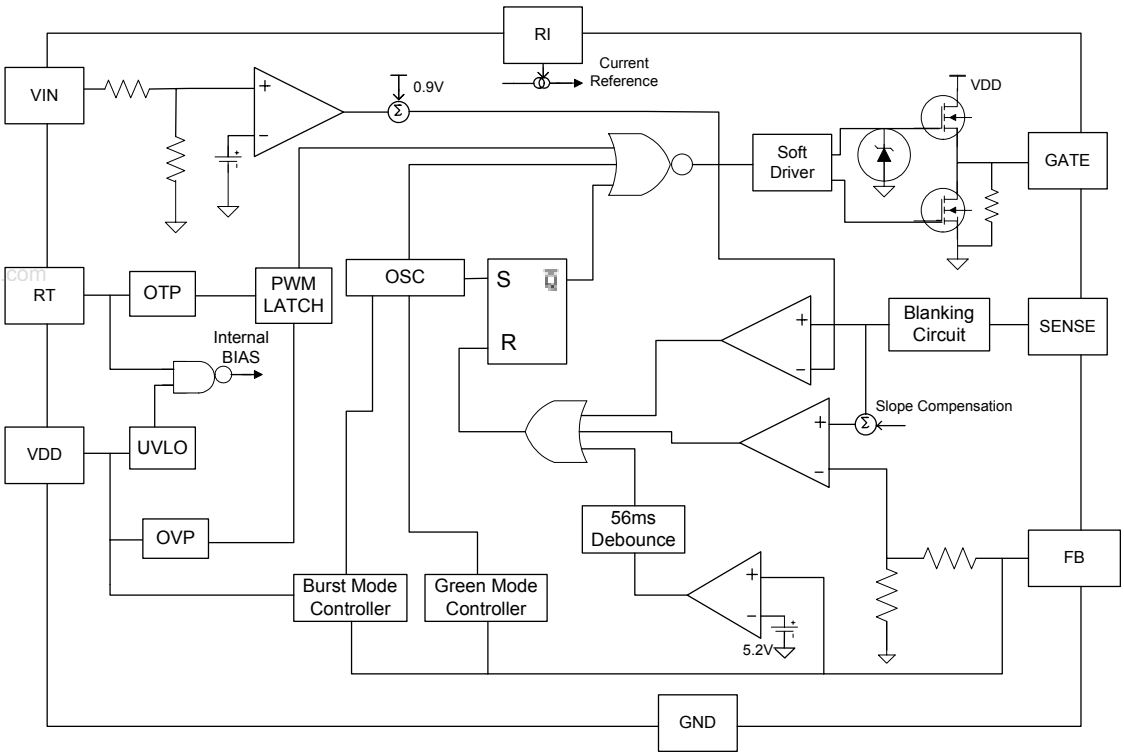



| Name | Description |
|---|---|
| GND | GND Pin |
| FB | Voltage feedback pin. The PWM duty cycle is determined by FB and Sense. |
| VIN | This pin is pulled high to the rectified line input through a large resistor for start-up. This pin is also used to detect line voltage to compensate for constant output power limit for universal AC input. |
| RI | By connecting a resistor to ground to set the switching freq.. Increasing the resistor will reduce the switching freq.. |
| RT | An NTC resistor is connected from this pin to ground for over-temperature protection. |
| SENSE | Current sense pin, The sensed voltage is used for current-mode control and pulse-by-pulse current limiting. |
| VDD | Power supply voltage pin. |
| GATE | Gate drive output to drive the external MOSFET.A soft driving waveform is implemented to improve EMI. |

## Typical Application Circuit



## Block Diagram






## Absolute Maximum Ratings

| Symbol | Parameter | | Rating | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage Pin Voltage | | 40 | V |
| $V_{FB}$ | Input Voltage to FB Pin | | -0.3 to 6V | V |
| $V_{Sense}$ | Input Voltage to SENSE Pin | | -0.3 to 6V | V |
| $P_D$ | Power Dissipation | | 1000 | mW |
| | ESD Capability, HBM Model | | 2000 | V |
| | ESD Capability, Machine Model | | 200 | V |
| $T_L$ | Lead Temperature(Soldering) | DIP-8（10sec）<br>SOP-8（10sec） | 260<br>230 | ℃<br>℃ |
| $T_{STG}$ | Storage Temperature Range | | -55 to + 150 | ℃ |

**Electrical Characteristics (**Ta=27°C unless otherwise noted, $V_{DD}$ = 15V.**)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Supply Voltage ($V_{DD}$ Pin)** | | | | | | |
| $I_{ST}$ | Startup Current | VDD=17 | | 7.5 | 30 | μA |
| $I_{SS}$ | Operating Current | $V_{FB}$= $V_{SENSE}$ = 0V VDD=15 | | 3.0 | 5 | mA |
| $V_{TH(ON)}$ | Start Threshold Voltage | -- | 16.0 | 16.5 | 17.0 | V |
| $V_{TH(OFF)}$ | Min. Operating Voltage | -- | 10.4 | 10.8 | 11.2 | V |
| VDD-OVP | VDD Over Voltage Protection(Latch off) | | 23.0 | 24.5 | 25.0 | V |
| VDD-th-g | VDD Low-Threshold Voltage to Exit Green-OFF Mode | | 11.0 | 12.0 | 13.0 | V |
| **Voltage Feedback (FB Pin)** | | | | | | |
| $I_{FB}$ | Short Circuit Current | $V_{FB}$=0V | | | 1.42 | mA |
| $V_{FB}$ | Open Loop Voltage | $V_{FB}$=Open | | 6.00 | | V |
| **Current Sensing (SEN Pin)** | | | | | | |
| $V_{TH}$ | Threshold voltage for current limit | $I_{VIN}$ =0 | | 0.76 | 0.9 | V |
| $T_{PD}$ | Delay to Output | | | 115 | 200 | nsec |
| $Z_{CS}$ | Input Impedance | | | 13 | | KΩ |
| $B_{nk}$ | Leading Edge Blanking Time | | 260 | 354 | 460 | nsec |
| **Oscillator (RI Pin)** | | | | | | |
| $F_{OSC}$ | Frequency in nominal mode | RI=26KΩ | 63 | 67 | 70 | KHz |
| $F_{OSC-green}$ | Frequency in green mode | RI=26 KΩ | 25 | 27 | 29 | KHz |
| $V_N$ | Beginning of frequency reducing at FB Voltage | VDD=15V | 1.95 | 2.05 | 2.15 | V |
| $V_G$ | End of frequency reducing at FB voltage | VDD=15V | 1.50 | 1.54 | 1.60 | $V_G$ |
| | Frequency Temp. Stability | -30-85°C | | 5.0 | | % |
| **GATE Drive Output (GATE Pin)** | | | | | | |
| $V_{OL}$ | Output Low Level | $V_{DD}$=12V, $I_O$=50mA | | 0.32 | 0.60 | V |
| $V_{OH}$ | Output High Level | $V_{DD}$=12V, $I_O$=50mA | 7.2 | 8.00 | | V |
| $T_R$ | Rising Time | VDD=15V,$C_L$=1nF | 200 | 240 | 280 | ns |
| $T_F$ | Falling Time | VDD=13V,$C_L$=1nF | 30 | 80 | 90 | ns |
| $DC_{MAX}$ | Maximum Duty Cycle | | 84 | 86 | 88 | |
| **Over-Temperature Protection Section** | | | | | | |
| $I_{RT}$ | Output current of pin RT | RI=26KΩ | 65 | 70 | 75 | μA |
| $V_{OTP}$ | Threshold voltage for over-temperature protection. | | 1.00 | 1.05 | 1.10 | V |
| **RI Section** | | | | | | |
| $RI_{NOR}$ | RI Operating Range | | 15.5 | 26 | 36 | KΩ |
| $RI_{MAX}$ | Max RI value for Protection | | | 216 | | KΩ |
| $RI_{MIN}$ | | | | 6 | | KΩ |

## OPERATION DESCRIPTION

### Start-Up Current & Operating Current

The typical start-up current is only 8μA. This allows a high resistance, low-wattage start-up resistor to be used, to minimize power loss. A 1.5MOhms, 0.25W, start-up resistor and a 10μF/40V VDD hold-up capacitor would be sufficient for an AC/DC adapter with a universal input range.

The required operating current has been reduced to 3.4mA. This results in higher efficiency and reduces the VDD hold-up capacitance requirement.



### Green-Power Mode Operation

The proprietary green-power mode function provides off-time modulation to continuously decrease the PWM frequency under light-load conditions. To avoid acoustic-noise problem, the minimum PWM frequency set above 25KHz. This green-power mode function dramatically reduces power consumption under light-load and zero-load conditions. Power supplies using a CR6842 controller can easily meet even the most restrictive international regulations regarding standby power consumption.

### Oscillator Operation

A resistor connected from the RI pin to GND pin generates a constant current source for the CR6842 controller. This current is used to determine the center PWM frequency. Increasing the resistance will reduce PWM frequency. Using a 26KΩ resistor $R_I$ results in a corresponding 67KHz PWM frequency. The relationship between $R_I$ and the switching frequency is:

$$f_{PWM} = \frac{1742}{R_I(K\Omega)}(KHz)$$

CR6842 also integrates frequency jittering function internally. The frequency variation ranges from around 63KHz to 70KHz for a center frequency 67kHz. The frequency jittering function helps reduce EMI emission of a power supply with minimum line filters.

$$I_{RT} = \frac{70\mu A}{R_I(K\Omega)} * 26$$

### Leading Edge Blanking

Each time the power MOSFET is switched on, a turn-on spike will inevitably occur at the sense-resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period, the current-limit comparator is disabled, and it cannot switch off the gate drive.

### Under-Voltage Lockout (UVLO)

The turn-on/turn-off thresholds are fixed internally at 12.4V/16.5V. To enable a CR6842 controller during start-up, the hold-up capacitor must first be charged to 16.5V through the start-up resistor.

The hold-up capacitor will continue to supply VDD before energy can be delivered from the auxiliary winding of the main transformer. VDD must not drop below 12.4V during this start-up process. This UVLO

hysteresis window ensures that the hold-up capacitor can adequately supply VDD during start-up.

## Gate Output / Soft Driving

The CR6842 output stage is a fast totem pole gate driver. Cross-conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 18V Zener diode in order to protect the power MOSFET transistors from any harmful over-voltage gate signals. A soft driving waveform is implemented to minimize EMI.



## Slope Compensation

The sensed voltage across the current sense resistor is used for peak-current-mode control and cycle-by-cycle current limiting. The built-in slope compensation function improves power supply stability and prevents peak-current-mode control from causing sub-harmonic oscillations. Within every switching cycle, the CR6842 controller produces a positively sloped, synchronized ramp signal.

## Constant Output Power Limit

When the SENSE voltage across the sense resistor $R_S$ reaches the threshold voltage, the output GATE drive will be turned off following a small propagation delay $T_{PD}$. This propagation delay will result in an additional current proportional to $T_{PD}*V_{IN}/L_P$. The propagation delay is nearly constant regardless of the input line voltage $V_{IN}$. Higher input line voltages will result in larger additional currents. Thus, under high input-line voltages the output power limit will be higher than under low input-line voltages.

The output power limit variation can be significant over a wide range of AC input voltages. To compensate for this, the threshold voltage is adjusted by the current $I_{IN}$. Since the pin VIN is connected to the rectified input line voltage through the start-up resistor, a higher line voltage will result in a higher current $I_{IN}$ through the pin VIN.

The threshold voltage decreases if the current $I_{IN}$ increases. A small threshold voltage will force the output GATE drive to terminate earlier, thus reducing total PWM turn-on time, and making the output power equal to that of the low line input. This proprietary internal compensation feature ensures a constant output power limit over a wide range of AC input voltages (90VAC to 264VAC).

## VDD Over-voltage Protection

VDD over-voltage protection has been built in to prevent damage due to over voltage conditions. When the voltage VDD exceeds the internal threshold due to abnormal conditions, PWM output will be turned off. Over-voltage conditions are usually caused by open feedback loops.

## Limited Power Control

The FB voltage will increase every time the output of the power supply is shorted or over-loaded. If the FB voltage remains higher than a built-in threshold for longer than $T_{LPS}$, PWM output will then be turned off. As PWM output is turned off, the supply voltage VDD will also begin decreasing.

When VDD goes below the turn-off threshold (eg, 12.4V) the controller will be totally shut down. VDD

will be charged up to the turn-on threshold voltage of 16.5V through the start-up resistor until PWM output is restarted. This protection feature will continue to be activated as long as the over-loading condition persists. This will prevent the power supply from overheating due to over loading conditions.

## Thermal Protection

An external NTC thermistor can be connected from the RT pin to ground. A fixed current $I_{RT}$ is sourced from the RT pin. Because the impedance of the NTC will decrease at high temperatures, when the voltage of the RT pin drops below 1.065V, PWM output will be disabled. The RT pin output current is related to the PWM frequency programming resistor $R_I$

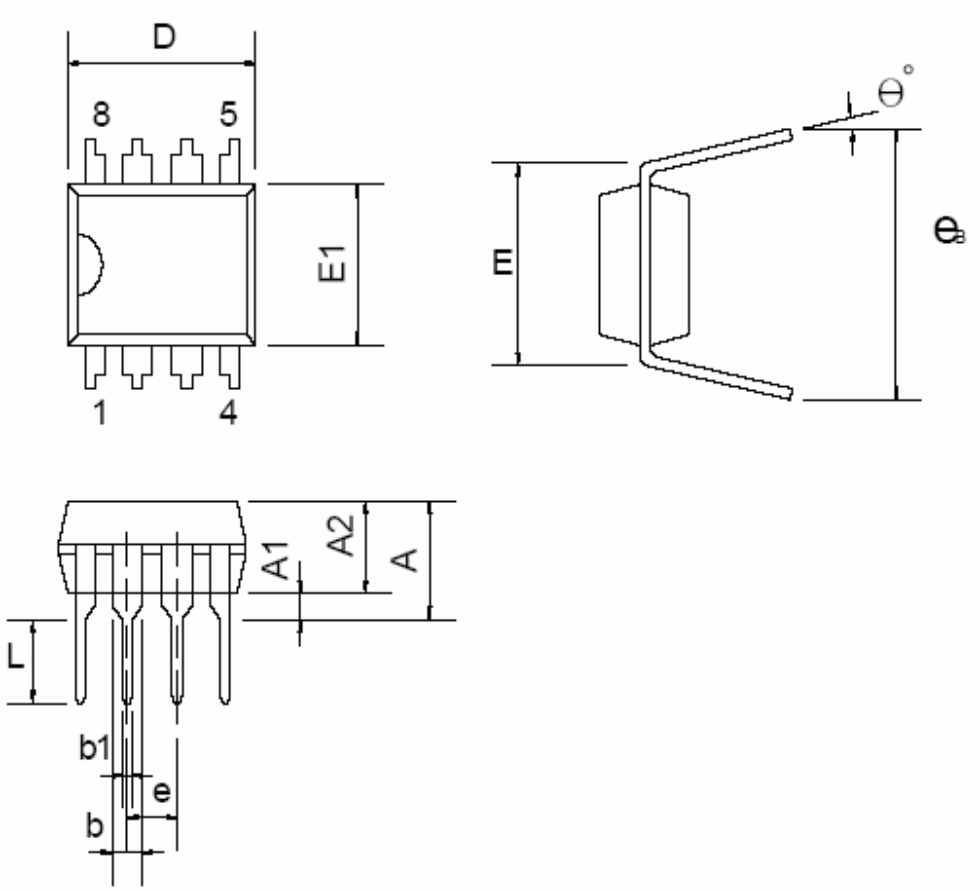


## Noise Immunity

Noise from the current sense or the control signal may cause significant pulse width jitter, particularly in continuous-conduction mode. Slope compensation helps alleviate this problem. Good placement and layout practices should be followed. The designer should avoiding long PCB traces and component leads. Compensation and filter components should be located near the CR6842. Finally, increasing the power-MOS gate resistance is advised.

## PACKAGE INFORMATION

### DIP-8L

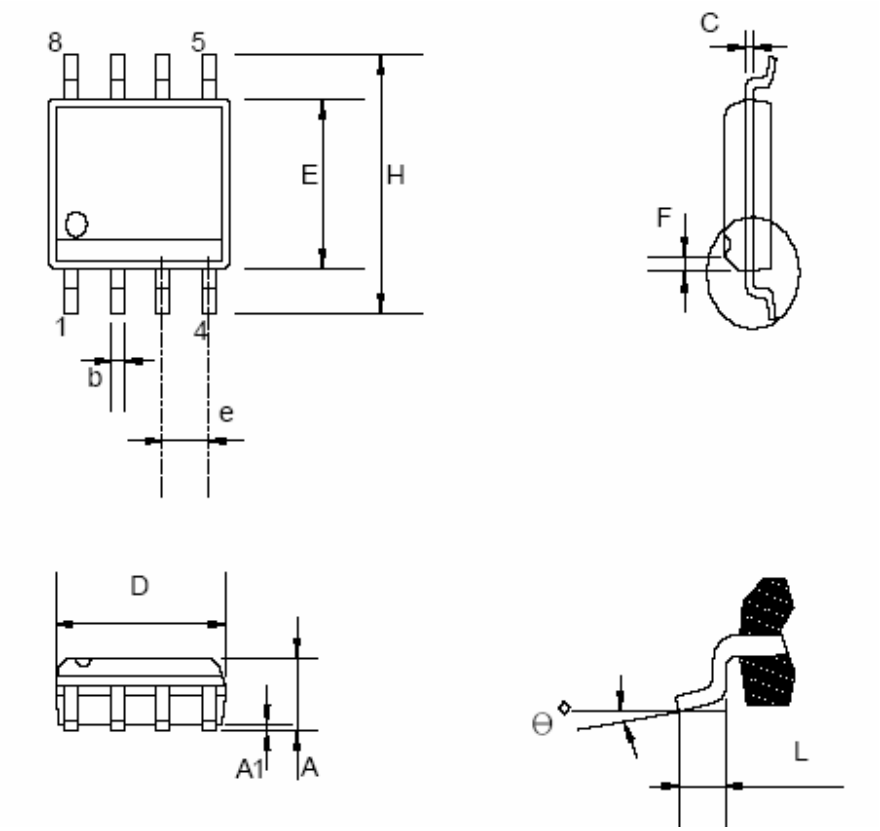





### Dimensions

| Symbol | Millimeters | | | Inches | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 5.334 | | | 0.210 |
| A1 | 0.381 | | | 0.015 | | |
| A2 | 3.175 | 3.302 | 3.429 | 0.125 | 0.130 | 0.135 |
| b | | 1.524 | | | 0.060 | |
| b1 | | 0.457 | | | 0.018 | |
| D | 9.017 | 9.271 | 10.160 | 0.355 | 0.365 | 0.400 |
| E | | 7.620 | | | 0.300 | |
| E1 | 6.223 | 6.350 | 6.477 | 0.245 | 0.250 | 0.255 |
| e | | 2.540 | | | 0.100 | |
| L | 2.921 | 3.302 | 3.810 | 0.115 | 0.130 | 0.150 |
| eB | 8.509 | 9.017 | 9.525 | 0.335 | 0.355 | 0.375 |
| θ° | 0° | 7° | 15° | 0° | 7° | 15° |

## SOP-8L






### Dimensions DISCLAIMERS

| Symbol | Millimeter | | | Inch | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 1.346 | | 1.752 | 0.053 | | 0.069 |
| A1 | 0.101 | | 0.254 | 0.004 | | 0.010 |
| b | | 0.406 | | | 0.016 | |
| c | | 0.203 | | | 0.008 | |
| D | 4.648 | | 4.978 | 0.183 | | 0.196 |
| E | 3.810 | | 3.987 | 0.150 | | 0.157 |
| e | 1.016 | 1.270 | 1.524 | 0.040 | 0.050 | 0.060 |
| F | | 0.381X45° | | | 0.015X45° | |
| H | 5.791 | | 6.197 | 0.228 | | 0.244 |
| L | 0.406 | | 1.270 | 0.016 | | 0.050 |
| θ° | 0 ° | | 8 ° | 0 ° | | 8 ° |